OUTLINE

- Introduction
- The CMOS Technology
- Layout of MOS Transistors
- Layout of Resistors
- Layout of Capacitors

INTRODUCTION

- Integrated Circuit: single component including a large number of active and passive devices and their interconnections to realize complex functions
- Monolithic Technology: all devices are realized on the same silicon crystal
- Planar Technology: all processing steps act on a very thin surface layer of the wafer
  - ☺ all IC's on the same wafer are realized simultaneously
  - ☺ fabrication costs are largely reduced

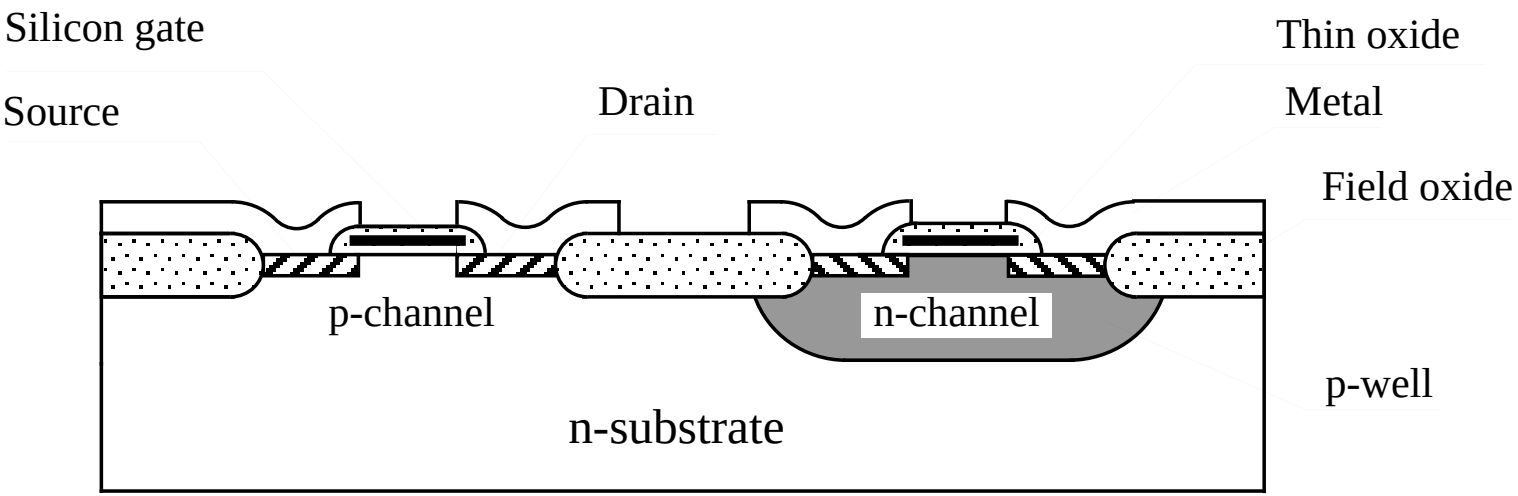
PROCESSING STEPS

- Modification of surface electrical characteristics of the wafer or deposition of films of various materials
  - thermal oxidation
  - ion implantation
  - thermal diffusion
  - epitaxy
  - film deposition
- Photolithographic processes
  - masking
  - selective etching

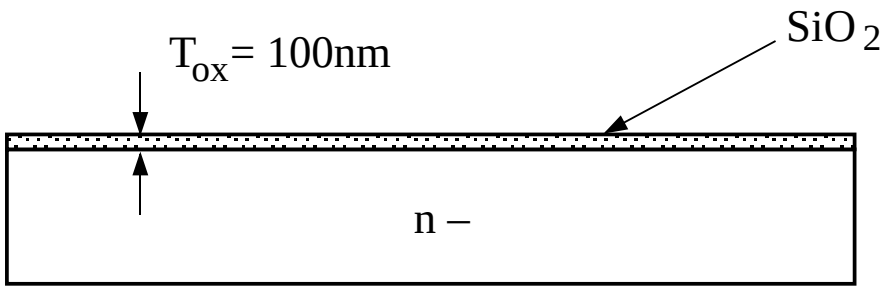
THE CMOS TECHNOLOGY

Available devices:

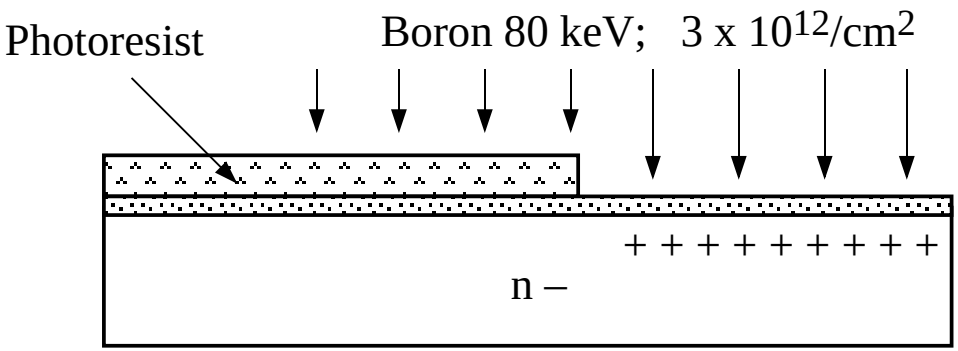
– n-channel MOS transistors
– p-channel MOS transistors
– resistors
– capacitors
– diodes (typically used for ESD protection)
– vertical bipolar transistors



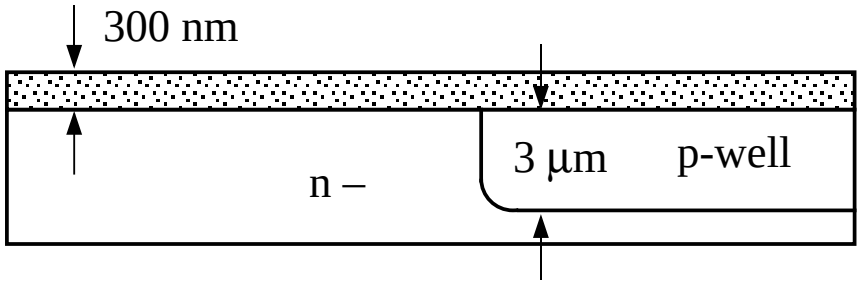
TYPICAL CMOS P-WELL PROCESS



– thermal oxidation

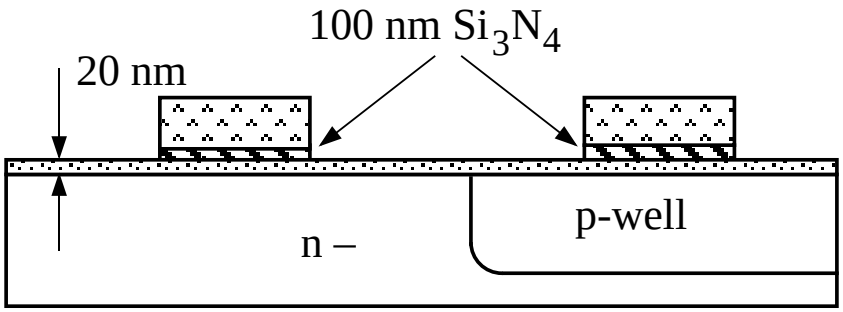


– p-well implant

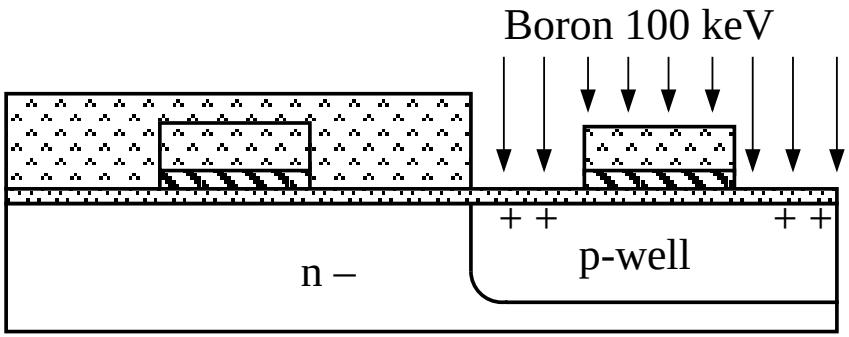


– p-well diffusion
– oxidation

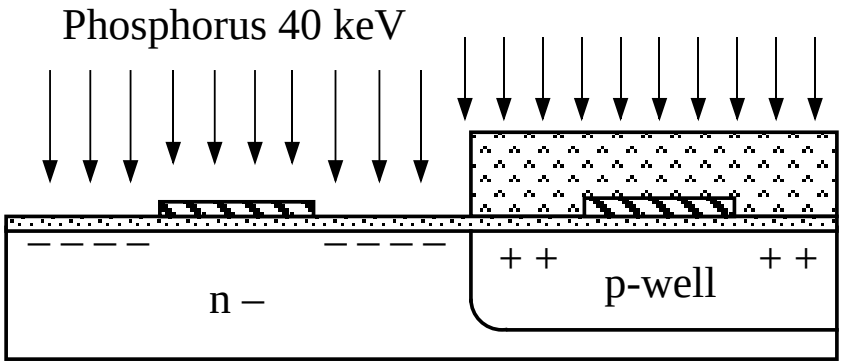
TYPICAL CMOS P-WELL PROCESS



– thin oxide growth
– active area definition

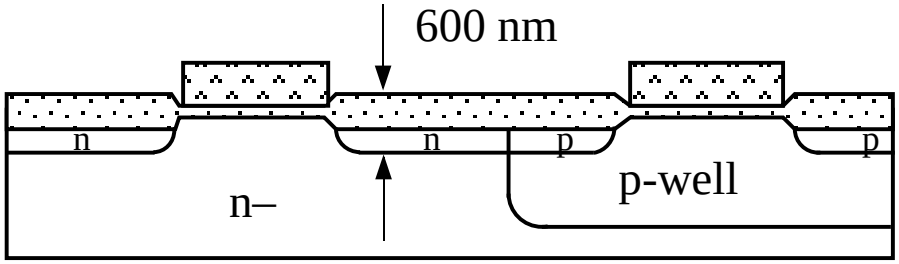


– p-implant isolation

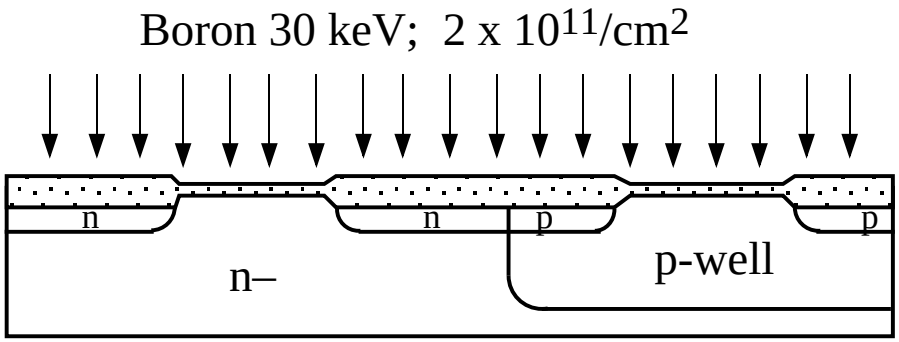


– n-implant isolation

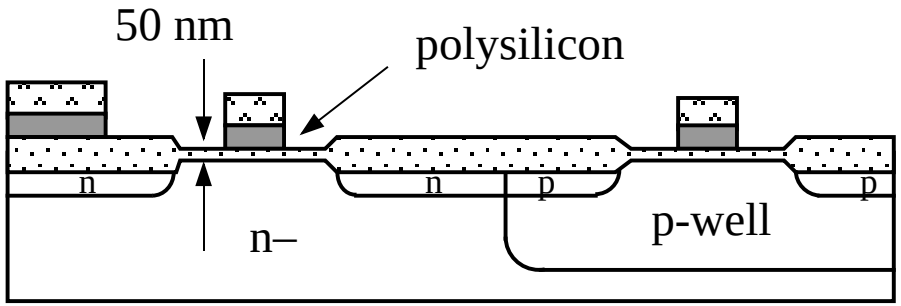
TYPICAL CMOS P-WELL PROCESS



– field oxide growth

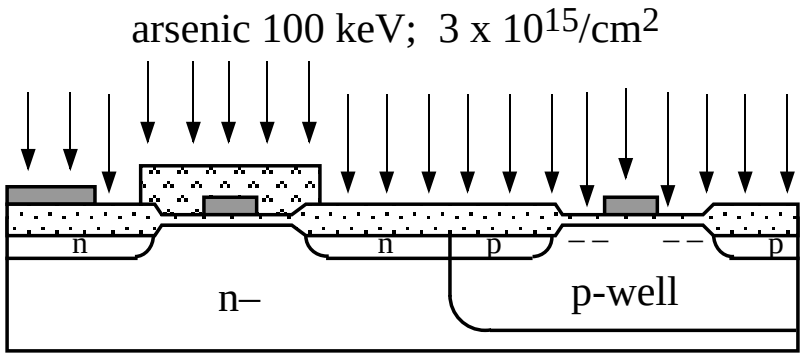


– additional implant to adjust threshold voltages

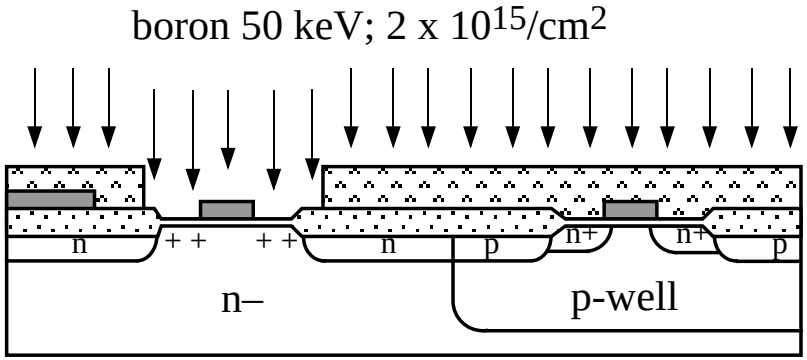


– definition of polysilicon gates and capacitor bottom plates

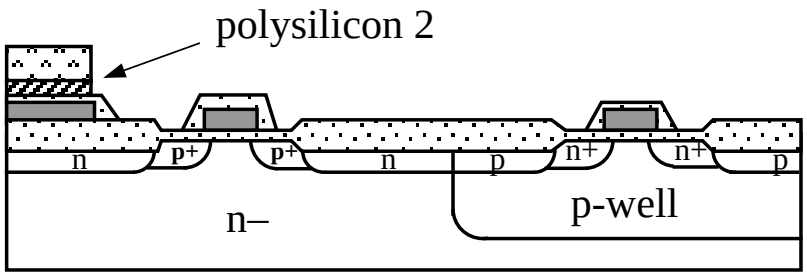
TYPICAL CMOS P-WELL PROCESS



– n-channel source & drain implant and diffusion

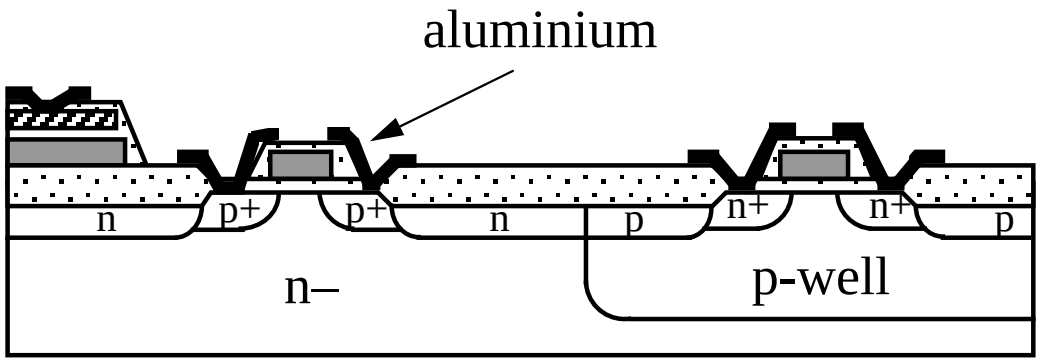


– p-channel source & drain implant and diffusion



– definition of capacitor top plate

TYPICAL CMOS P-WELL PROCESS



– contact opening
– metal deposition

possibly:
– thermal oxidation
– via opening
– second metal layer deposition

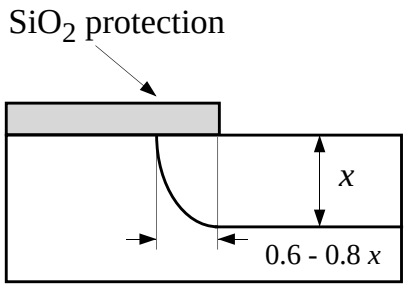
– final passivation using silicon nitride (Si_3N_4) (typical thickness 1 µm)

DIFFERENCES LAYOUT - CIRCUIT

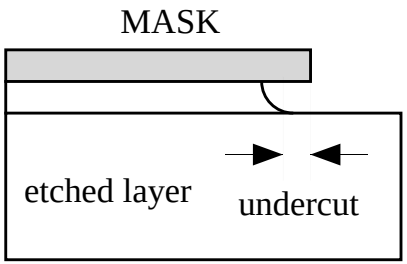
Why a designed layout and its corresponding real circuit are different?

- lateral diffusion
- etching under protection
- boundary dependent etching
- three-dimensional effects

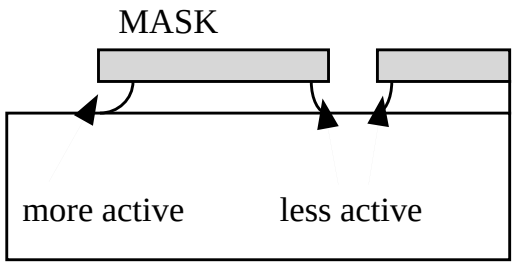
and the errors and limitations associated with mask production and mask alignment.



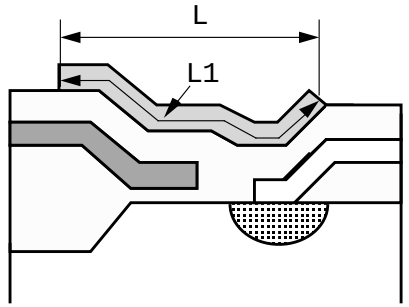
LATERAL DIFFUSION



ETCHING UNDER PROTECTION



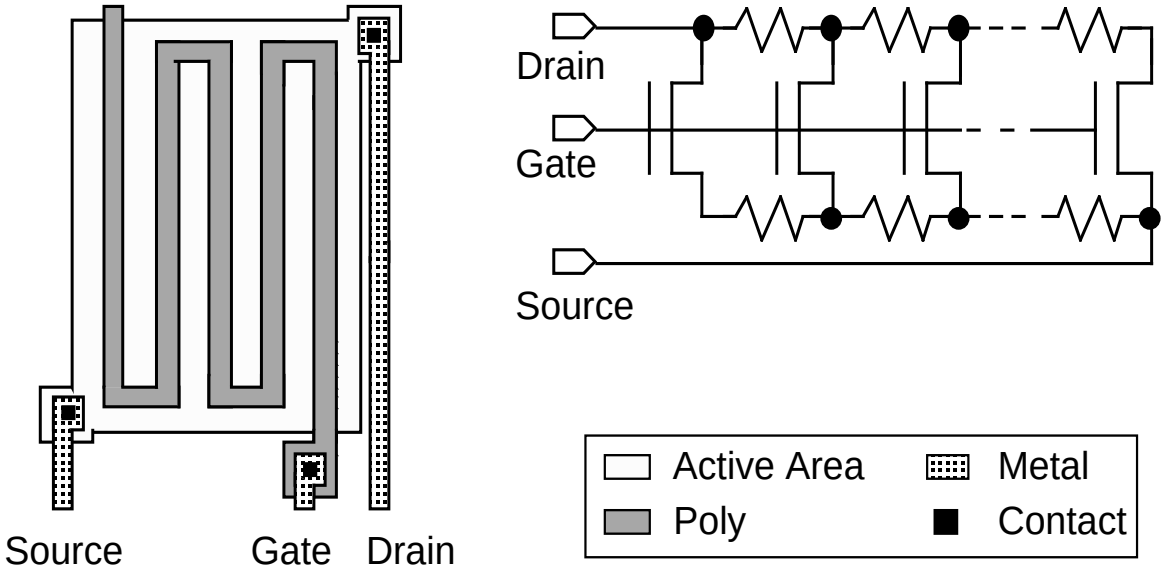
BOUNDARY DEPENDENT ETCHING



THREE-DIMENSIONAL EFFECTS

LAYOUT OF MOS TRANSISTORS

- In the layout of a digital transistor the speed, the load driving capability and the area optimization are key issues
- Matching, accurate aspect ratio (W/L), noise are not very important



Extreme situation of a layout of a *digital* transistor

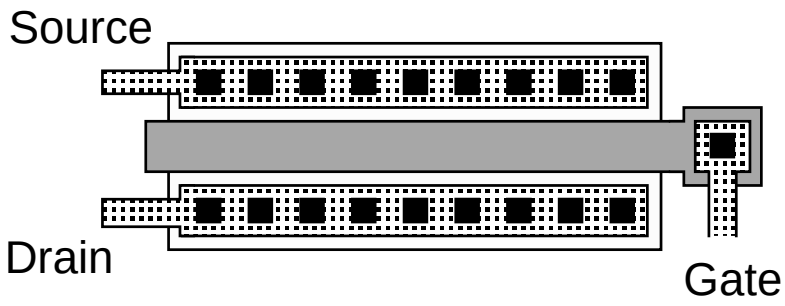
LAYOUT OF MOS TRANSISTORS

In the layout of analog transistors it is important to:

- ❒ have an accurate aspect ratio (straight structures)
- ❒ minimise the stray resistance in series with source and drain
- ❒ reduce the gate series resistance

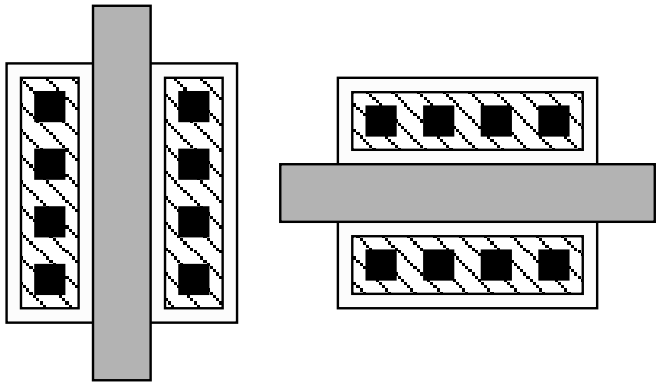
For wide transistors it is worthwhile to split the layout into the parallel connection of many elements (stacked configuration)

Layout of an *analog* transistor

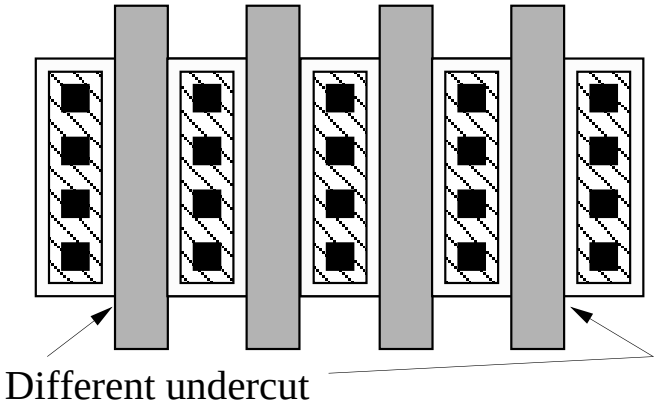


TRANSISTOR MATCHING

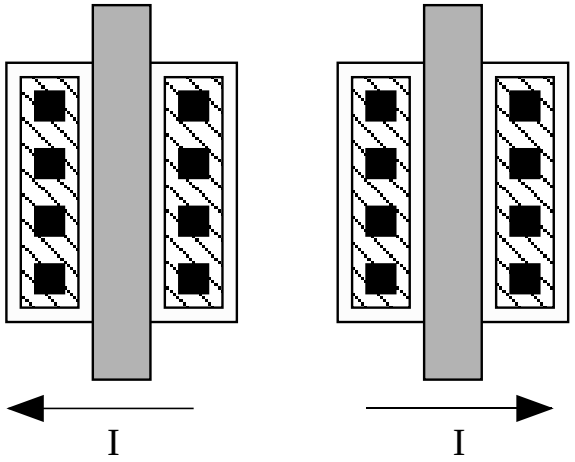
Orientation



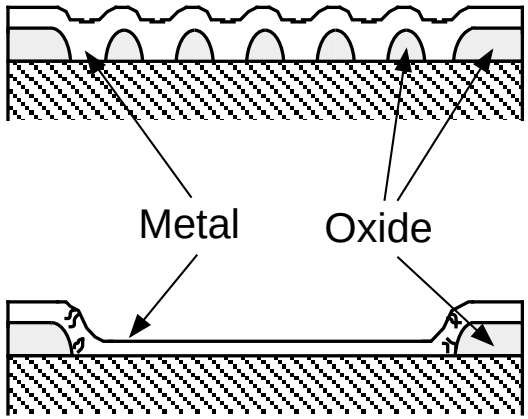
Boundary conditions



Current flow direction

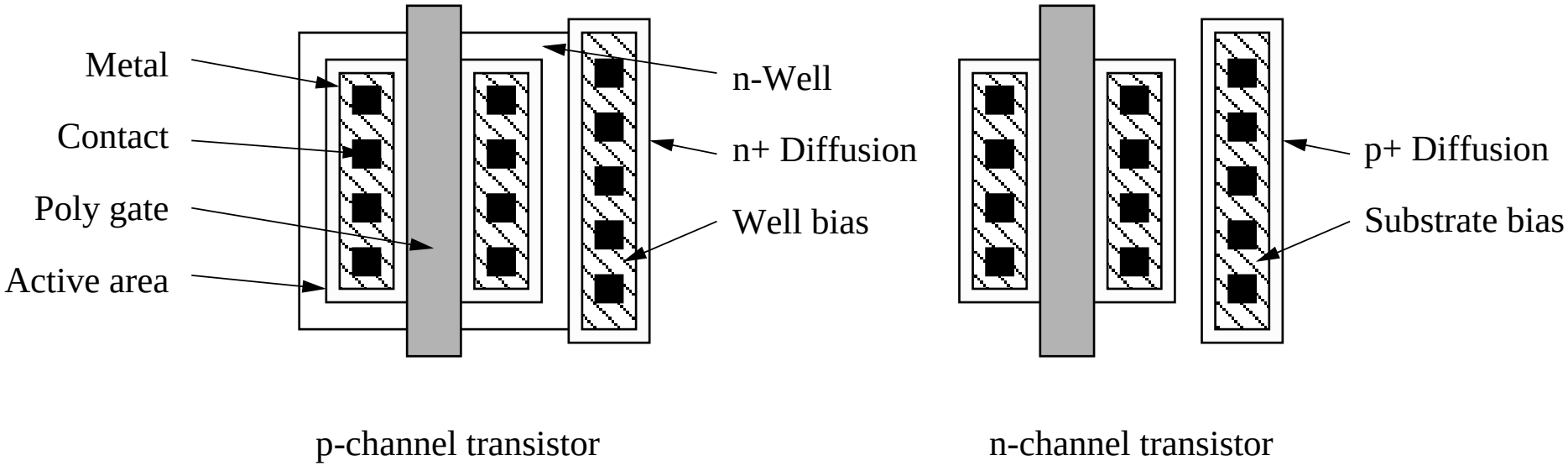


Multiple contacts (reliability issue)



SUBSTRATE BIASING

- Biasing must be as close as possible to the active devices
- Any noisy signal affecting the substrate or the well should be sinked by the biasing and not affecting the circuit itself



ABSOLUTE & RELATIVE ACCURACIES

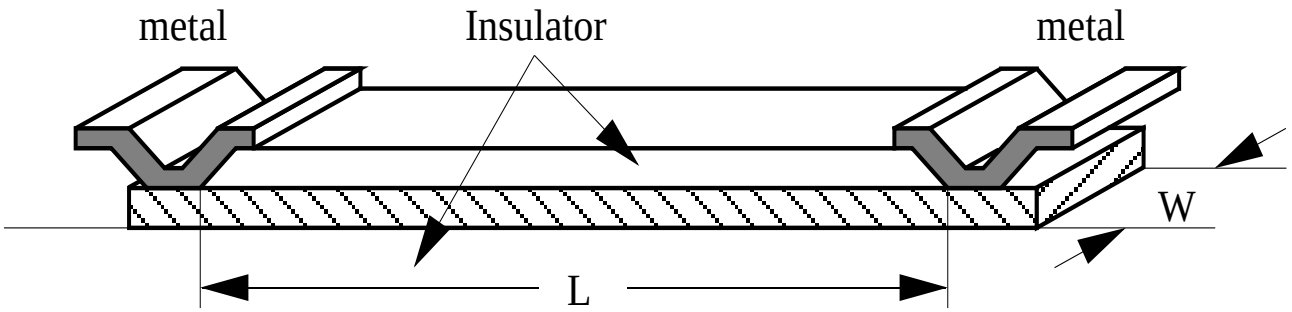
Transistor's parameters

Parameter	Symbol	Typical value	Absolute accuracy	Matching accuracy
threshold	V_{th}	0.8 V	0.2 V	5 mV (100µm dist.)
mobility (n)	μ_n	463 cm^2/V sec	15 %	1 % (100µm dist.)
mobility (p)	μ_p	167 cm^2/V sec	15 %	1 % (100µm dist.)
oxide cap.	C_{ox}	2.16 fF/μm^2	6 %	0.1 % (100µm dist.)
length	L	–	0.3 µm	0.04 µ (20µm dist.)
width	W	–	0.3 µm	0.04 µ (20µm dist.)

LAYOUT OF RESISTORS

Integrated resistors are made of thin strips of resistive layer

- a resistive strip is contacted at the two terminals by ohmic contacts (metal – p+ or n+)
- insulation from the surrounding is made by oxide layers or by reversely biased junctions

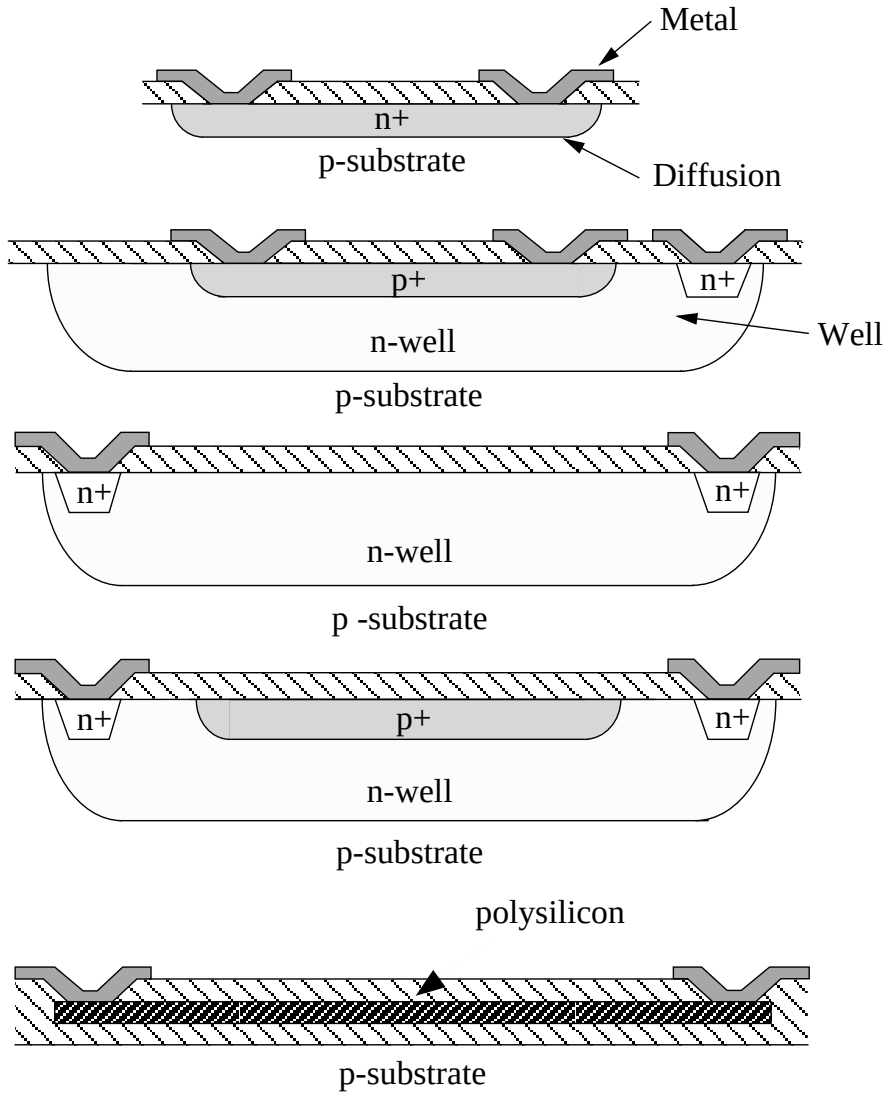


$$R = 2R_{cont} + \frac{L}{W}R_{\square} = 2R_{cont} + \frac{\rho}{x_j}\frac{L}{W}$$

$R_{\square}$ sheet resistance

LAYOUT OF RESISTORS

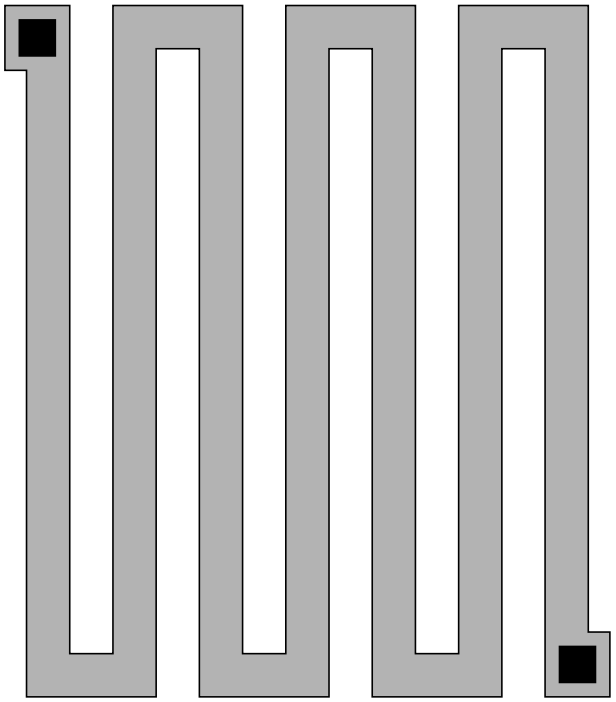
- n+ diffusion
- p+ diffusion
- n-well
- pinched n-well
- polysilicon



ACCURACY OF RESISTORS

The sheet resistance is pretty low →long strips must be used

Serpentine shapes are commonly used

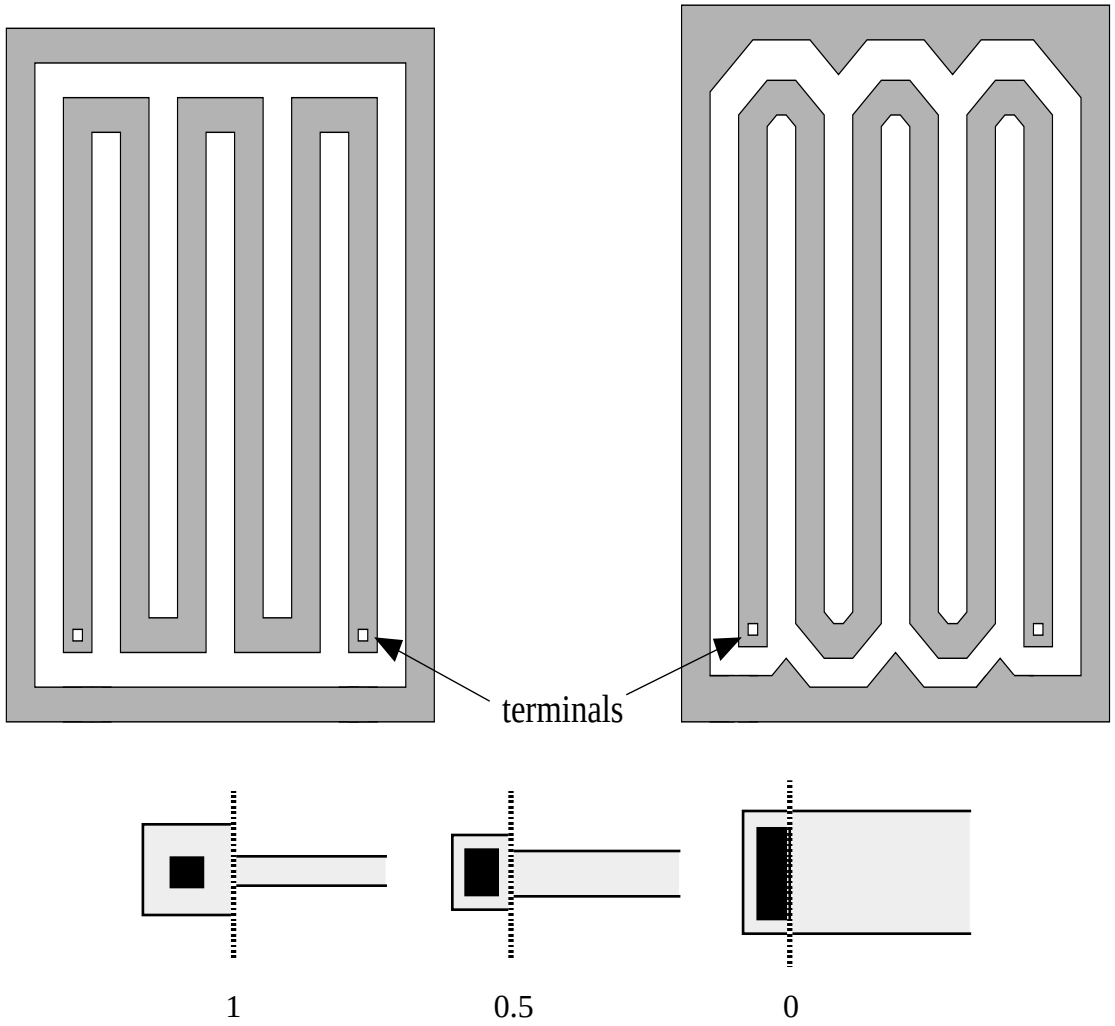


- Problems of corners (estimated half a square)
- Undercut (width reduction)
- Boundary dependent undercut
- Parameter's gradient

$$\left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \rho}{\rho}\right)^2 + \left(\frac{\Delta x_j}{x_j}\right)^2$$

LAYOUT OF ACCURATE RESISTORS

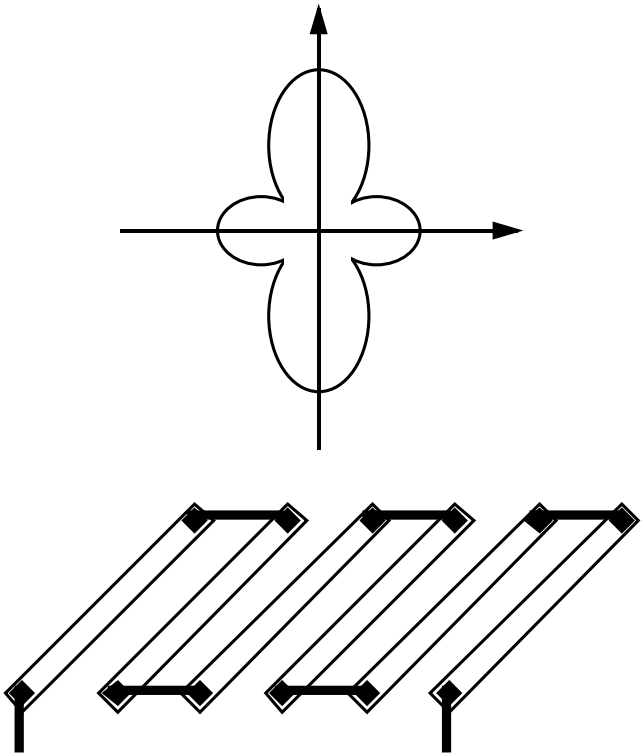
- Use of rounded or 45° corners
- Use of dummy strips to get the same boundaries
- Large width to limit the random component of the undercut
- Suitable endings



FACTORS AFFECTING ACCURACY

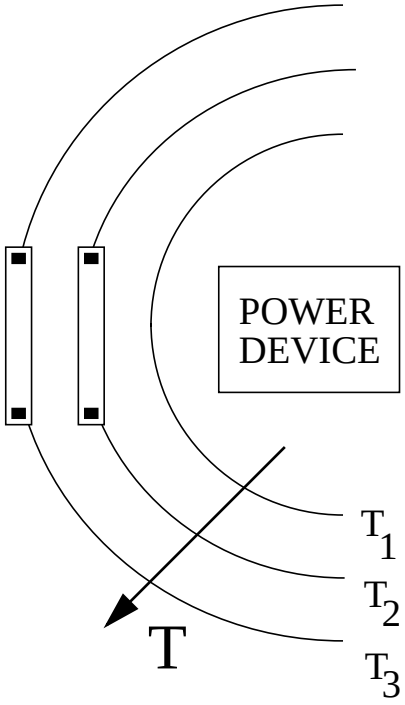
Stress

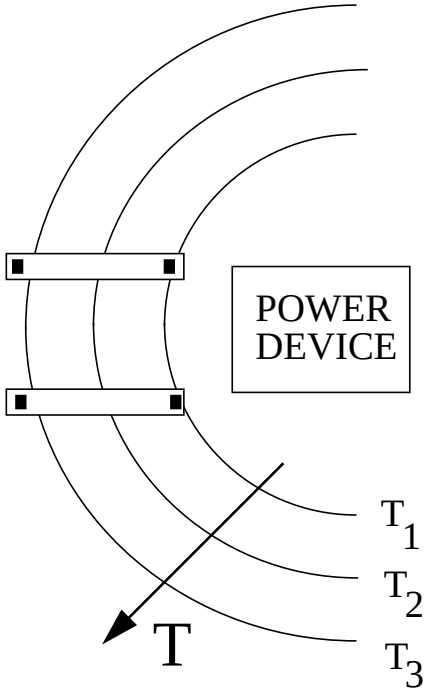
Variation is anisotropic
Minimum at 45°



Temperature

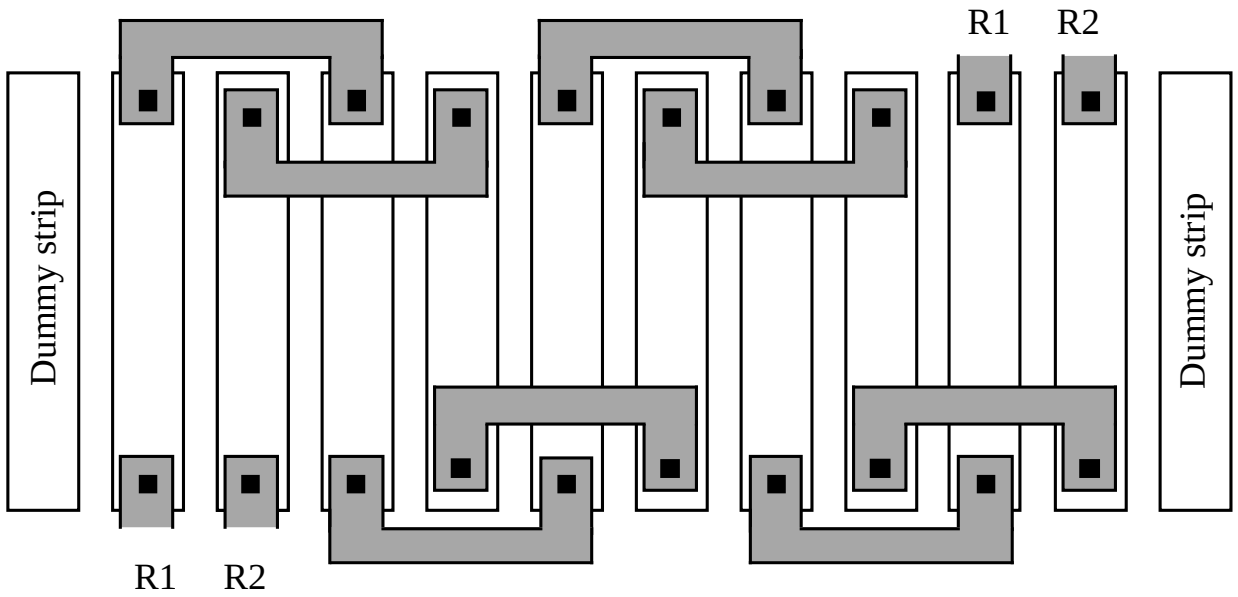
Temp. gradients affect accuracy
Elements symmetrical with respect to the power device





INTERDIGITIZED RESISTORS

- Absolute accuracy is poor because of the large parameter drift
- Ratio or matching accuracy is better because it depends on the local variation of parameters
- Use of interdigitized structures (common centroid) minimizes errors due to gradient in the parameters value

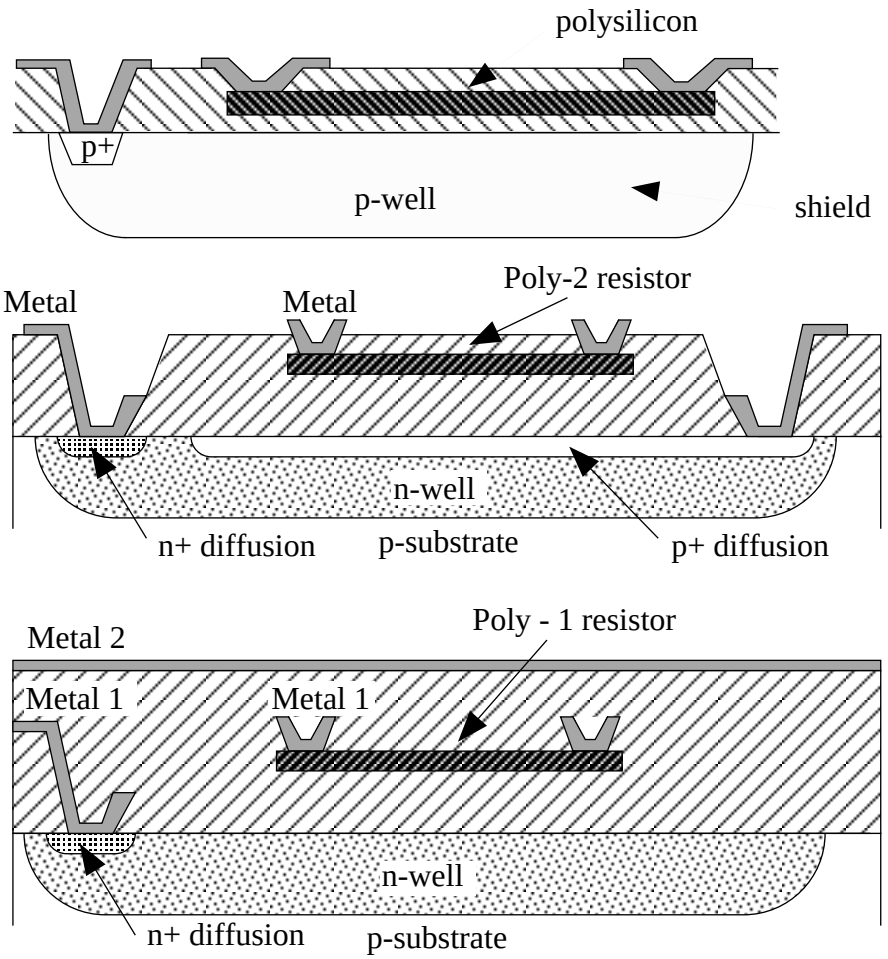


RESISTOR FEATURES

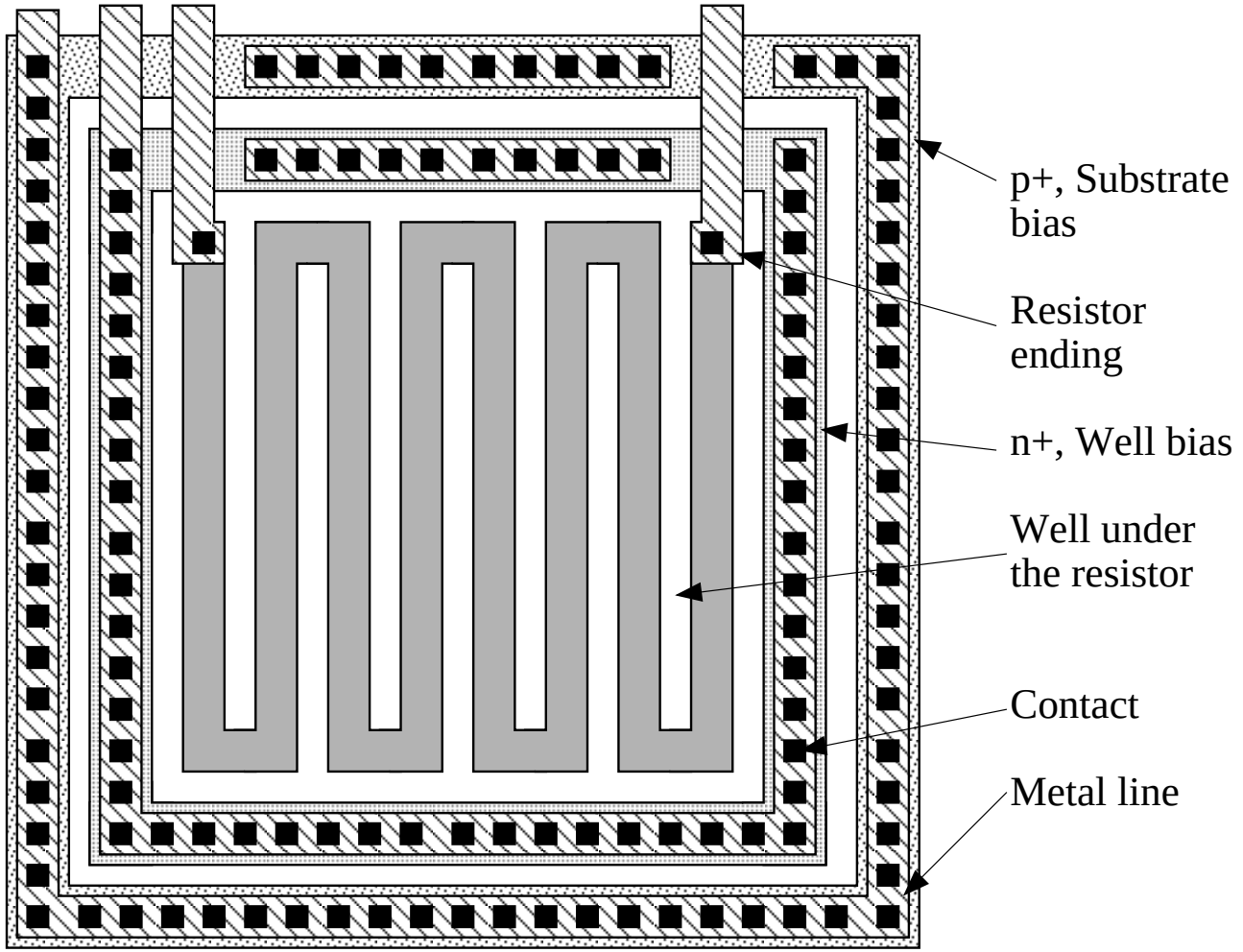
Type of layer	Sheet Res. Ω/□	Accuracy %	Temp. C. ppm/°C	Volt. C. ppm/V
n+ diff	20-35	20-40	1800	50-300
p+ diff	25-60	20-40	1700	50-300
n-well	1K-1.4K	15-30	6.5K	10K
p-well	3K-6K	15-30	6.5K	10K
pinch. n-well	6K-10K	25-40	10K	20K
pinch. p-well	9K-13K	25-40	10K	20K
first poly	20-28	15-30	900	20-200
second poly	21-33	15-30	800	20-200

SHIELDING

- Mixed analog-digital systems are affected by the problem of noisy interference between the analog and the digital sections
- The most critical source of coupling are the resistances
- It is important to guarantee possible shielding toward the substrate (or possibly the top side)



SHIELDING


p+, Substrate bias
Resistor ending
n+, Well bias
Well under the resistor
Contact
Metal line

RESISTOR GUIDELINES

For matching:

- use of equal structures
- not too narrow ($W > W_{min}$)
- interdigitize
- thermal effect compensation
- 45° orientation if stressed

For good TC:

- use of n+ or p+ layers
- use of poly layers

For absolute value:

- use of diffused layers; suitable endings

INTEGRATED CAPACITORS

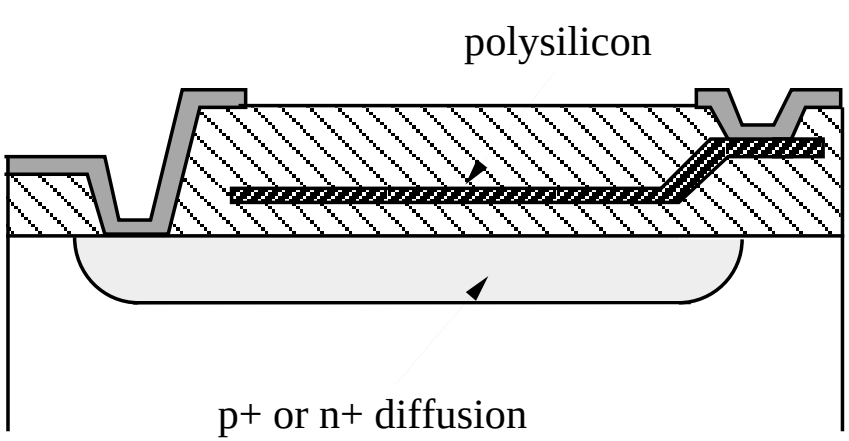
Electrodes: metal, polysilicon, diffusion
Insulator: silicon oxide, polysilicon oxide, CVD oxide

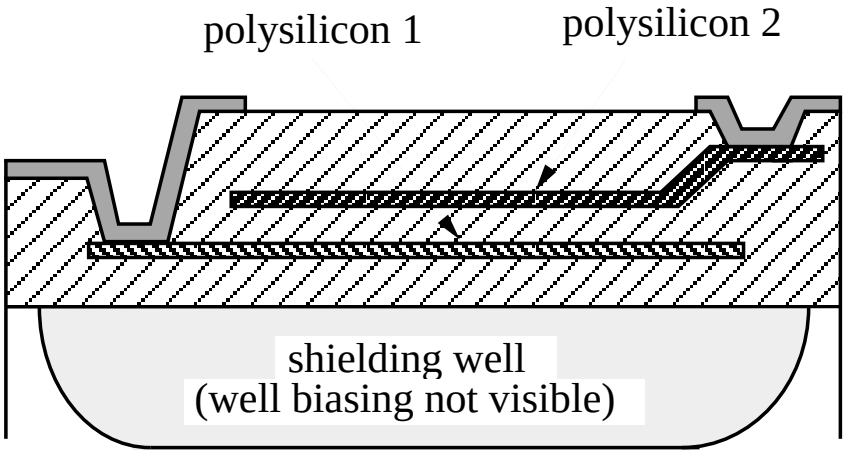
$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

t_{ox} = 16 nm

C = 2.16 fF/μm^2

➢ A “normal” capacitance is 1 pF

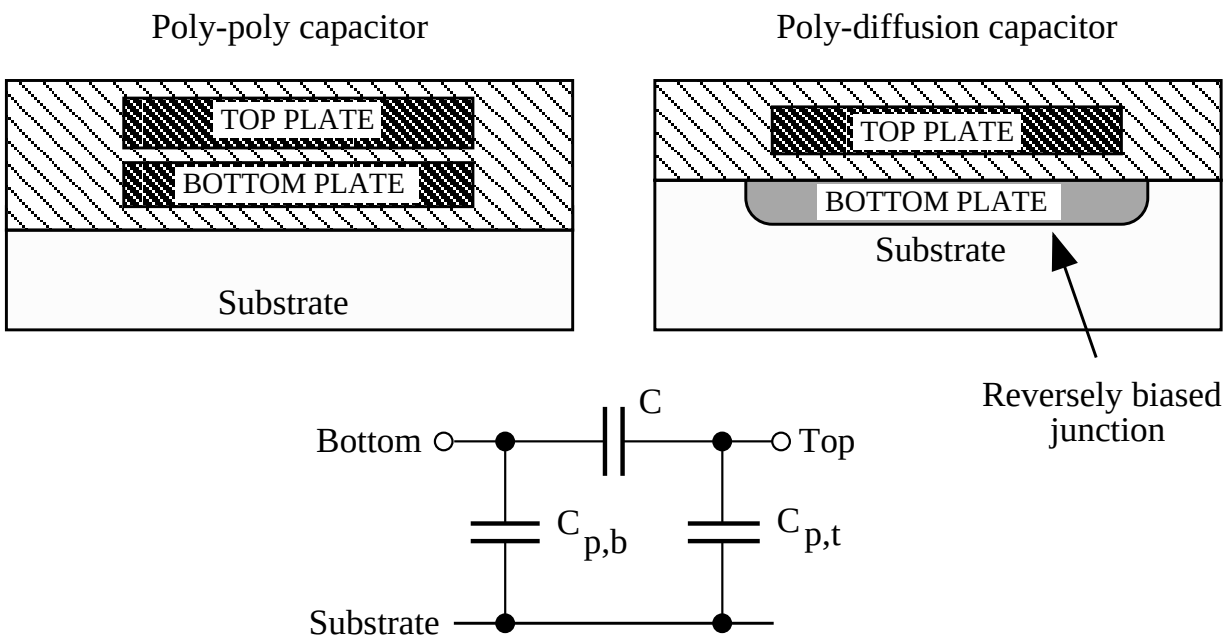




INTEGRATED CAPACITORS

Integrated capacitors are made by structures very close to the silicon substrate

➢ parasitic capacitances are not negligible and affect any integrated capacitor



Poly-poly capacitor:

$C_{p,b} = 0.01\ C$

$C_{p,t} = 0.001\ C$

Poly-diff capacitor:

$C_{p,b} = 0.1\ C$

$C_{p,t} = 0.01\ C$

INTEGRATED CAPACITORS ACCURACY

$$\sigma_C^{\,2} = \left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

$\frac{\delta \varepsilon_r}{\varepsilon_r}$:

- oxide damage
- impurities
- stress
- temperature
- bias condition
- bias history (for CVD)

$\frac{\delta L}{L}; \frac{\delta W}{W}$:

- etching
- alignment

$\frac{\delta t_{ox}}{t_{ox}}$:

- oxide grow rate
- poly grain size

UNDERCUT EFFECT

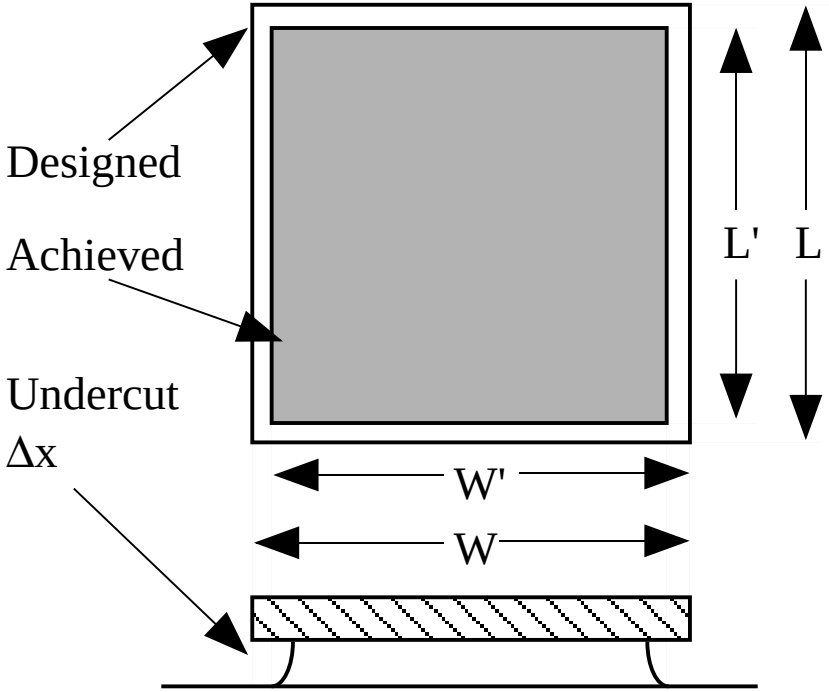
The value of the area is given by the smaller plate or by the thin oxide area (fringing components are neglected)

The actual area is less than the designed area because of the undercut effect

$$A' = W'L' \cong WL - 2(L + W)x$$

$$A' \cong A\left(1 - \frac{P}{A}x\right)$$

the same proportional reduction if the perimeter-area ratio is kept constant

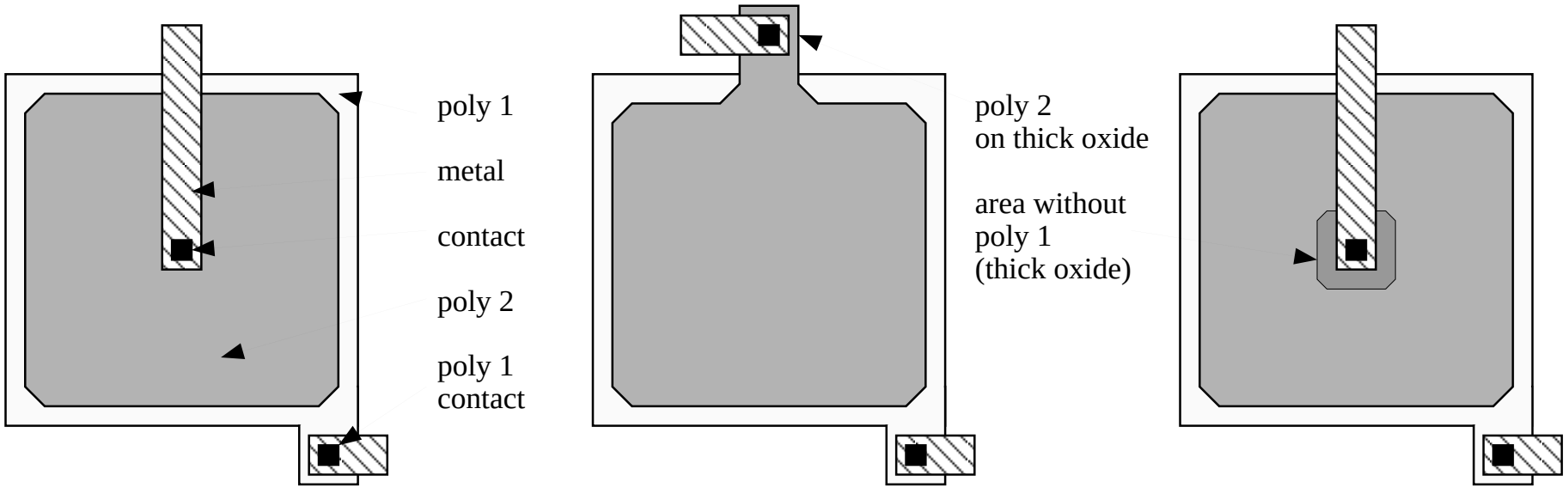


$$W' = W - 2x$$

$$L' = L - 2x$$

LAYOUT OF CAPACITORS

- Capacitors are used as matched elements to define precise ratios
- They are often connected to the virtual ground of op-amps
  - ➢ careful layout matching
  - ➢ good shielding to limit injection of noisy signals

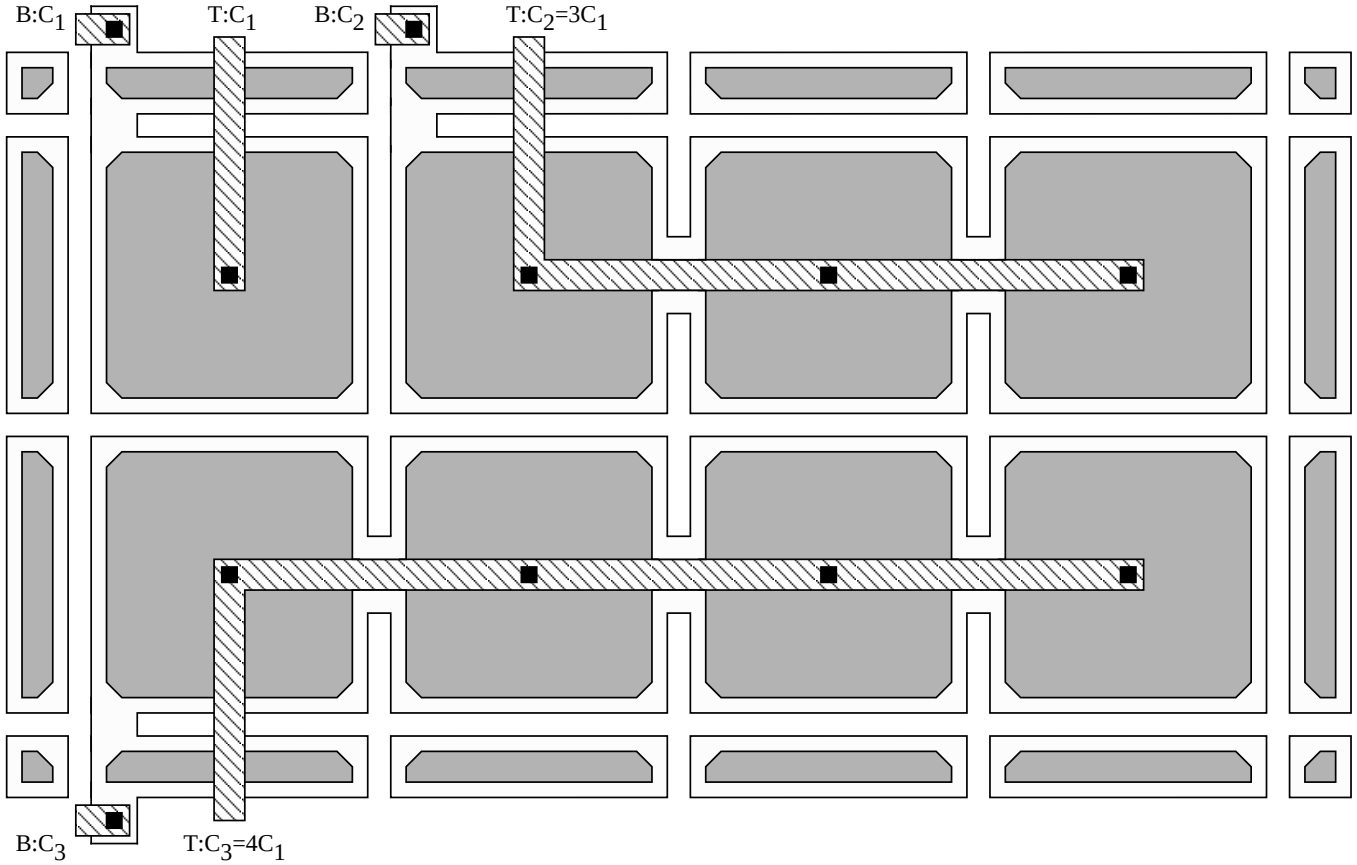


CAPACITOR FEATURES

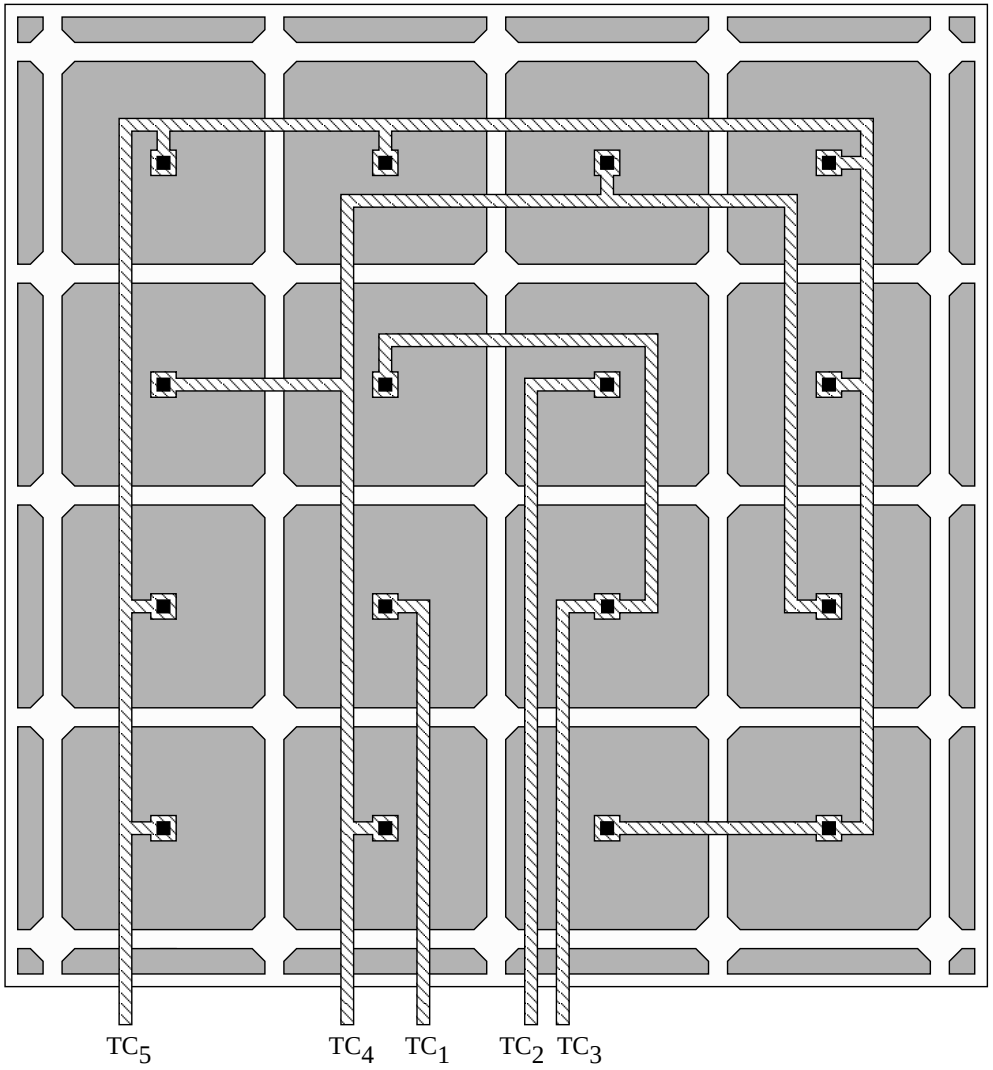
Type	t_{ox} nm	Accuracy %	Temp. C. ppm/°C	Volt. C. ppm/V
poly-diff	15-20	7-14	20-50	60-300
poly1-poly2	18-21	6-12	20-50	40-200
metal-poly	600-700	6-12	50-100	40-200
metal-diff	1200-1400	6-12	50-100	60-300
metal1-metal2	750-1250	6-12	50-100	40-200

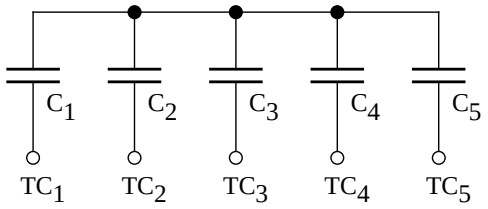
CAPACITOR MATCHING

- Matched capacitors should have the same perimeter-area ratio
- Unity capacitors must be used



COMMON CENTROID ARRANGEMENT





$$C_2 = C_1$$
$$C_3 = 2C_1$$
$$C_4 = 4C_1$$
$$C_5 = 8C_1$$