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POWER DEVICES AND SYSTEMS LABORATORY

Exercise 5P

Static Properties of Power Transistors

High-Voltage Bipolar Junction Transistor

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Exercise Introduction

1. Exercise Aim and Plan

The aim of this exercise is to investigate and compare static properties of different power transistors: the BJT (a single one and a Darlington one), the MOSFET and the IGBT. This will provide a fuller understanding of why all three device types are still present on the market, each one in its own field of application. Using a dedicated power device curve tracer, appropriate characteristics will be recorded. From the recorded images, data for the on-state will be extracted and used to calculate power losses as a function of load (missing parameters will be read out from device datasheets). Based on the results obtained, the different devices will be compared between them in respect of their applicability depending on load current as well as on power loss and drive power requirements.

This exercise is also an occasion to investigate in more detail the power bipolar junction transistor (BJT). This is because its advantages are particularly prominent in the aspect of principal circuit static properties.

Selected information on physical phenomena taking place in semiconductor structures, especially on conduction mechanisms, will be useful in this exercise; they are covered in Manual 0, Refs. I and J. Brief descriptions of MOSFET and IGBT structures and properties are given in Manual 0, Ref. H (that also covers the BJT), whereas more detailed analyses can be found in references listed in Manuals 3P and 4P, respectively.

2. Power Bipolar Junction Transistors

2.1. Recommended reading

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
A	Ben	6, 6.1, 6.2.1, 6.2.2, 6.3.2	2.2, 2.3, 2.4		
B	Ben	6.5	2.5		

Additionally, from Manual 0 references:

Ref.	Textbook	Excerpt	Equivalent in the Polish Manual	Complementary Reading	Complements in this Manual
0 H	Ben	3.1.2	2.1		

3. Practical Significance of Static Parameters of Transistors

3.1. Principal parameters of power semiconductor devices

3.1.a. Power semiconductor device key absolute maximum parameters

The bipolar junction transistor was the first transistor to have a high-voltage structure developed. It presented several drawbacks, which led to the invention of the power MOSFET. The disadvantages of the latter were in turn an inspiration for the development of some better performing devices (in certain respects) such as the IGBT.

However, as it can be noticed, MOSFETs and BJTs are still present on the market. This follows from the simple fact that engineers still apply them in power converter circuits they design. If psychological factors such as habits and resistance to changes are put aside, one must conclude that older devices must still have better properties in some aspects or application fields. One only has to determine what specific aspects and fields they are.

When talking about fields of application of power semiconductor devices, this term may be understood either in the circuit context (in what circuits a given device can be favourably applied; however, this would require some knowledge about the operation of these circuits), or in the device context, i.e. what requirements for parameter values a given device is able to fulfil. Three principal, easy to compare, maximum admissible parameters are usually considered:

(1) voltage (voltage capability),

(2) current (absolute maximum current),

(3) frequency (maximum switching frequency).

It should always be remembered that power semiconductor devices operate as switches in most applications, i.e. components switched at a given frequency between the off-state (blocking) and the on-state (conducting).

3.1.b. Frequency

The maximum operating frequency of a semiconductor switch results from its dynamic parameters. They are, first of all, the turn-on and turn-off times and (as a consequence) the energies dissipated during turn-on and during turn-off.

Dynamic phenomena or parameters are not the object of this exercise. In these respects, the particular transistors to be investigated can be briefly characterised as follows:

— **MOSFETs**, as unipolar devices, are much faster than all the bipolar devices;

— **IGBTs** virtually turn on as fast as MOSFETs, but they exhibit a particularly long and energetically unfavourable turn-off (related to the current tail) even though this drawback is quite successfully minimised at present;

— **BJTs**, as a strictly bipolar device, shows relatively long switching times;

— **the Darlington BJT** is the slowest one.

3.1.c. Voltage

The voltage capability of power semiconductor devices results from parameters of the lightly doped layer included in their structures. These parameters determine the breakdown voltage of a junction which sustains the high voltage.

In the above respect, technological possibilities are similar for each of the considered transistors. Differences arise from physical and electrical limitations:

— for unipolar transistors any improvement in voltage capability is connected with an increase in their on-state resistance (which is a consequence of decreasing the dopant concentration and increasing the longitudinal dimension of the lightly doped layer);

— for bipolar devices any improvement in voltage capability is connected with an increase in switching times (which is a consequence of increasing the longitudinal dimension of the lightly doped layer and increasing the excess carrier lifetime therein with the intention of reducing the on-state resistance); and for the BJT, additionally, with a decrease in current gain (a decrease of the transport coefficient α_t due to the lengthening of the distance to be travelled by charge carriers).

Consequently, it is commercially profitable to manufacture transistors with voltage capabilities of the following orders of magnitude (in the case of silicon devices):

— for MOSFETs, up to a few hundreds of volts;

— for IGBTs, up to a few kilovolts;

— for (single) BJTs, up to kilovolts, but only for weak currents, while just tens (or a hundred) volts for strong currents.

3.1.d. Current

The maximum current that a given component can conduct is related to the capability of conducting heat out of the semiconductor structure, this heat resulting from the current flow itself. A more intensive energy dissipation requires a larger, more durable and more complex casing. Usually, it is necessary to apply additional cooling components (heat sinks), and frequently, forced cooling as well (fans, fluid circulation) and even semiconductor forced cooling (micro-channels with cooling fluid realised in the semiconductor substrate). This of course affects the cost of applying the considered device.

Thus, it is power loss that in fact lies under the concept of current capability. The total power loss in a device is composed of the principal circuit power loss P_{loss} and the control power, i.e. the power used in the control circuit, P_{ctrl}:

$$P_{\text{tot}} = P_{\text{loss}} + P_{\text{ctrl}} \tag{3.1}$$

In the case of current-controlled transistors, the control power may be comparable to (or even greater than) the principal circuit power loss. In such a case, the P_{ctrl} component cannot be neglected in the analysis of a transistor's safe operation conditions, as this power is also dissipated in the device, producing thermal effects. However, in order to simplify the analysis and to enable comparisons between different devices, we will limit our considerations to the principal circuit power loss. This power loss in the static on-state equals

$$P_{\text{loss}} = I_{\text{o}} \cdot U_{\text{on}}(I_{\text{o}}, X_{\text{ctrl}}) \tag{3.2}$$

where I_{o} is the load current flowing through this device's principal circuit and U_{on} is the voltage dropped between its main terminals by the flowing current.

The U_{on} voltage mainly depends on the principal current but, to some extent, also on the control quantity X_{ctrl}. Depending on the particular device, this control quantity (in a static state) may be a current I_{ctrl} or a voltage U_{ctrl}. As the load is normally forced by an external circuit (and is therefore independent of the device itself), it is the on-state voltage U_{on}, at a given current and under given control conditions, that constitutes the main indicator of a device's applicability.

Let us assume that the current flowing through a transistor has a pulse waveform with a zero base. The transistor is therefore conducting for some part t_p (the pulse width) of the switching period T_s and is blocking for the remaining part thereof. The related duty cycle is

$$D = \frac{t_p}{T_s} \tag{3.3}$$

In addition, let us assume that the off-state power loss is negligible as compared to the on-state power loss. Taking into account that only static properties are analysed in the present exercise, let us consider a frequency low enough for the power loss in dynamic states to be negligible as well.

Under the above assumptions, the instantaneous power loss will have a pulse waveform with a pulse width equal t_p and an amplitude expressed with Eq. (3.2). The resulting principal circuit average power loss is, by definition:

$$P_{loss} = \frac{1}{T_s}\int_{T_s} p_{loss}(t)\mathrm{d}t = \frac{1}{T_s}\left(\int_{t_p} I_o U_{on}\mathrm{d}t + \int_{T_s - t_p} 0\mathrm{d}t\right) = \frac{1}{T_s} I_o U_{on} t_p = D I_o U_{on} \tag{3.4}$$

However, power is an issue not only as considered in the macroscale (when it is attributed to the entire device treated as a lumped object), but also in the microscale (when it is analysed inside the semiconductor structure, which in fact has a distributed character). In practice, not a single point of the semiconductor structure can be allowed to overheat. This in turn makes it necessary to consider the power density instead:

$$p_v = \frac{\Delta P}{\Delta V} = J^2 \rho \tag{3.5}$$

where $\Delta V \to 0$ is the volume of the considered structure segment wherein a certain amount ΔP out of the total power is generated, J is the current density inside this segment and ρ is the resistivity inside this segment, resulting from carrier concentration.

If decreasing resistivity is not possible, then power density is minimised by decreasing current density. Under the assumption that the structure is homogenous and that the current flow is uniform, current density is:

$$J = \frac{I_o}{A} \tag{3.6}$$

where I_o is the total current conducted in the device (along its principal circuit) and A is the total cross-section area (perpendicular to the current flow direction) of the structure. However, increasing the silicon wafer area can sometimes be economically inefficient as it raises the cost of the wafer itself and that of the casing.

3.2. Control criterion

3.2.a. Control power

Until now, we have only considered parameters related to the principal circuit. However, the control mechanism and the power necessary to control a device (control power) are also important factors influencing the applicability of different power semiconductor devices.

Power transistors may be controlled using one of two mechanisms: current control or voltage and charge control (see Manual 0, Ref. H). We will now describe both of them from the quantitative point of view.

Assuming that the drive current source is ideal, the drive power is equal to the power loss in the transistor's input circuit is

$$p_{\mathrm{ctrl}} = i_{\mathrm{ctrl}} u_{\mathrm{ctrl}} \tag{3.7}$$

where i_{ctrl} is the current in the control circuit (i.e. the control terminal current), u_{ctrl} is the control circuit voltage (i.e. the voltage between the control terminal and the common terminal).

3.2.b. Current control

It follows from the principle of current control that the control current flow is continuous, so the power loss in the on-state is constant and equals

$$P_{\mathrm{ctrl}} = I_{\mathrm{ctrl}} U_{\mathrm{ctrl}} \tag{3.8}$$

In the specific case of the BJT,

$$P_{\mathrm{ctrl}}(I_{\mathrm{C}}, I_{\mathrm{B}}) = I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) \tag{3.9}$$

To induce a pulse waveform of the principal current i_{o}, the control quantity i_{B} must also have a pulse waveform. Consequently, the instantaneous control power will have a pulse waveform, too, and its amplitude will be expressed with Eq. (3.9). In the off-state, $I_{\mathrm{B}} = 0$ as the base-emitter junction is unbiased or reverse biased. Thus, the average control power is:

$$\begin{aligned} P_{\mathrm{ctrl}}(I_{\mathrm{C}}, I_{\mathrm{B}}) &= \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} p_{\mathrm{ctrl}} \mathrm{d}t = \frac{1}{T_{\mathrm{s}}} \left(\int_{t_{\mathrm{p}}} I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) \cdot \mathrm{d}t + \int_{T_{\mathrm{s}} - t_{\mathrm{p}}} 0 \cdot \mathrm{d}t \right) = \\ &= \frac{t_{\mathrm{p}}}{T_{\mathrm{s}}} \cdot I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) = D \cdot I_{\mathrm{B}} \cdot U_{\mathrm{BE}}(I_{\mathrm{C}}, I_{\mathrm{B}}) \end{aligned} \tag{3.10}$$

Just as in the case of the principal circuit power loss, the increased power consumption in the dynamic states has been neglected. This results in an under-estimation of power which increases with increasing switching frequency.

3.2.c. Voltage and charge control

In this second case of device control, the current flow follows from charging and discharging the device's input capacitance. As this is a transient process, the control terminal current is variable in time and has the form of pulses occurring only in the turn-on and turn-off states.

The average control power is generally expressed with:

$$P_{\mathrm{ctrl}} = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} p_{\mathrm{ctrl}} \mathrm{d}t = \frac{1}{T_{\mathrm{s}}} \int_{T_{\mathrm{s}}} i_{\mathrm{ctrl}} u_{\mathrm{ctrl}} \mathrm{d}t \tag{3.11}$$

The forcing control voltage has a certain constant value equal to the steady-state input voltage U_{ctrl}. A current i_{ctrl} is only drawn from the source during the turn-on time interval (considered with respect to the gate circuit), $t_{\mathrm{on(G)}}$. Thus,

$$P_{\mathrm{ctrl}} = \frac{U_{\mathrm{ctrl}}}{T_{\mathrm{s}}} \int_{t_{\mathrm{on(G)}}} i_{\mathrm{ctrl}}(t)\mathrm{d}t \tag{3.12}$$

The integral of current is nothing else but a charge. The charge Q_{G} delivered to the transistor's gate during turn-on (as considered with respect to the gate circuit, i.e. over the time interval $t_{\mathrm{on(G)}}$) is called the total gate charge. Using this quantity, the Eq. (3.12) may be expressed as:

$$P_{\mathrm{ctrl}} = \frac{U_{\mathrm{ctrl}}}{T_{\mathrm{s}}} \cdot Q_{\mathrm{G}} = Q_{\mathrm{G}} U_{\mathrm{ctrl}} f_{\mathrm{s}} \tag{3.13}$$

where f_{s} is the switching frequency.

In the particular case of the MOSFET,

$$P_{\mathrm{ctrl}}(I_{\mathrm{D}}, U_{\mathrm{GS}}, f_{\mathrm{s}}) = Q_{\mathrm{G}}(I_{\mathrm{D}}, U_{\mathrm{GS}}) \cdot U_{\mathrm{GS}} \cdot f_{\mathrm{s}} \tag{3.14}$$

while for the IGBT,

$$P_{\mathrm{ctrl}}(I_{\mathrm{C}}, U_{\mathrm{GE}}, f_{\mathrm{s}}) = Q_{\mathrm{G}}(I_{\mathrm{C}}, U_{\mathrm{GE}}) \cdot U_{\mathrm{GE}} \cdot f_{\mathrm{s}} \tag{3.15}$$

3.2.d. Gate charge

The gate charge may be given in a transistor's datasheet as a single number. However, it should be taken into account that it is an increasing function of the control voltage U_{ctrl} (i.e. U_{GS} or U_{GE}) as well as an increasing function of the principal on-state current I_{o} (i.e. I_{D} or I_{C}). It is additionally an increasing function of the principal off-state voltage ($U_{\mathrm{DS(off)}}$ or $U_{\mathrm{CE(off)}}$); however, this relationship is relatively weak, so it will be neglected in the present exercise.

For a specific set of values of the above quantities, the gate charge value Q_{G} can only be read out from an appropriate gate charge characteristic. Fig. 1 presents an exemplary shape of this characteristic for a MOSFET transistor. For example, for a U_{GS} voltage of 10 V (and for the nominal principal current value, $I_{\mathrm{D(nom)}}$), one can read out the charge value of Q_{G} = 55 nC.

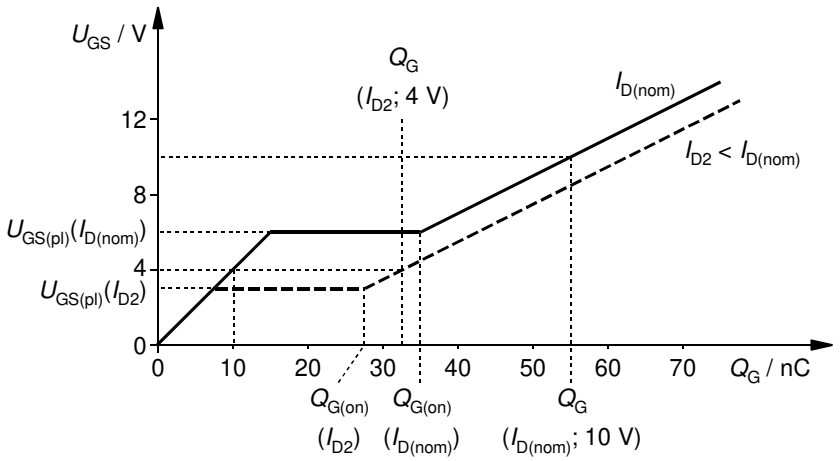


Fig. 1. Example gate charge characteristic used to determine the gate charge value Q_{G} for specific transistor operating conditions

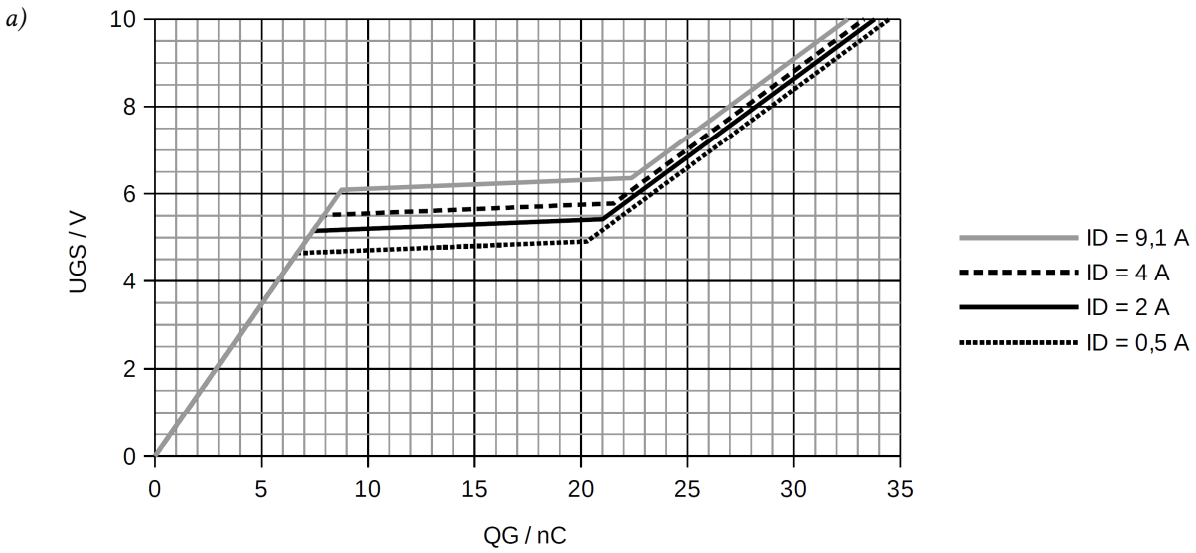
The effect of the principal current (the drain current I_{D} for a MOSFET) is often neglected in the gate charge characteristic. However, if the nominal value $I_{\mathrm{D(nom)}}$ for which the characteristic was obtained is considerably greater than the one appearing in the transistor's real operating circuit, this

may result in the value of Q_G being read out from the first rising section of this characteristic. This has been illustrated in in Fig. 1 for some current of I_{D2} and for the voltage of U_{GS} = 4 V, where a result of 10 nC would have been obtained. However, it follows from the analysis of the switching process that the transistor is turned on only at the (right) end of the horizontal section called the "plateau," where the control voltage has an almost constant value of $U_{GS(pl)}$. Therefore, the charge delivered to the transistor's gate during the turn-on time interval $t_{on(G)}$ can never be less than the value that corresponds to the second bend point, marked as $Q_{G(on)}$. In the considered example this is 35 nC for the current of $I_{D(nom)}$ and 27,5 nC for I_{D2}.

Had the characteristic been measured for the proper, lower current value of I_{D2}, the level of $U_{GS(pl)}$ would have been located below (the dashed curve in Fig. 1), so the readout would have been made from a point located on the second rising section, yielding Q_G = 32,5 nC, which is this parameter's true value.

However, if the characteristic for the real current value (I_{D2}) is not known and if this current significantly differs from the nominal one, then the gate charge can be determined in the following way:

(1) read a value of $U_{GS(pl)}$ for the current of I_{D2} from the transfer characteristic, $I_D = f(U_{GS})$;



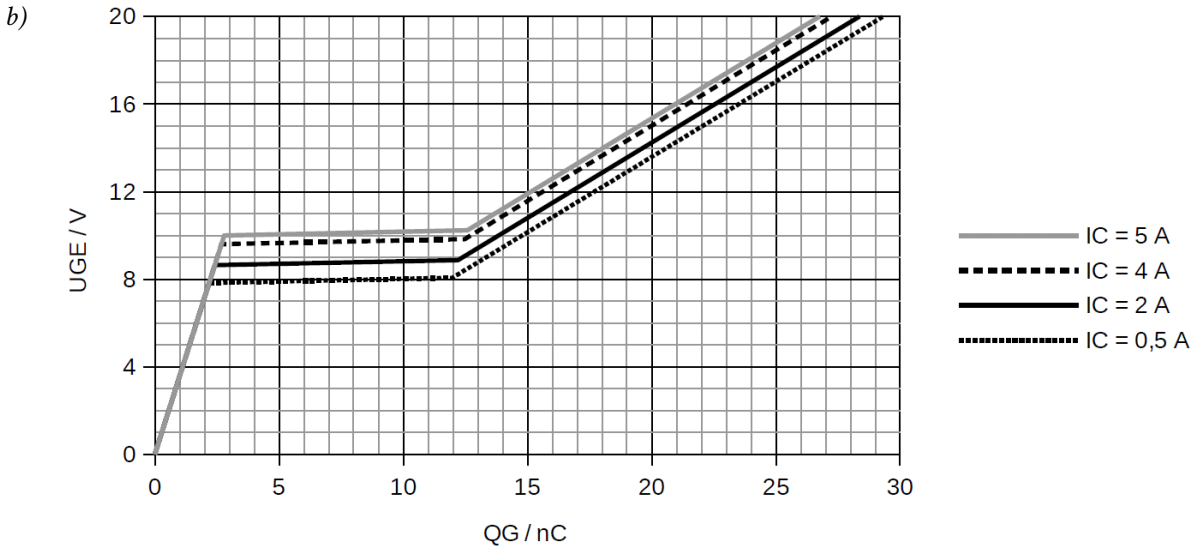


Fig. 2. Gate charge characteristic for the transistors under investigation in the present exercise for selected currents lower than nominal: a) IRFB9N60A MOSFET (at U_{DS} = 400 V); b) IRG4BC10K IGBT (at U_{CE} = 400 V)

(2) by geometrical construction, draw the gate charge characteristic for the current of I_{D2}, considering that from the operating principle of field-effect transistors and from the usual gate charge measurement method it follows that:
   - the slopes of the subsequent linear sections do not change (in fact, the slope of the plateau may slightly change, but this has to be ignored as this variation cannot be predicted based on data available in technical sheets; moreover, this slope is insignificant as compared to the other linear sections of the characteristic),
   - the length of the plateau (the Q_{GD} charge) does not depend on the I_D current (it depends on the principal turn-off voltage $U_{DS(off)}$),
   - to further simplify the task, the plateau may even be assumed to be horizontal;

(3) read the Q_G charge from the characteristic constructed.

Gate charge characteristics obtained by the above method for the MOSFET and the IGBT to be investigated in this exercise, for current values lower that the respective nominal ones have been presented in Fig. 2.

If a rough estimate of control power is sufficient, e.g. for a preliminary selection of a device for a given circuit, then it can be assumed that $Q_G = Q_{G(on)}(I_{D(nom)})$, which yields 35 nC in the analysed example. This is because at least an error of power underestimation is not committed this way. In any case, the value of 10 nC, which would result from reading out at the point of intersection with the first rising section, is unacceptable as totally unreal; as it can be seen by analysing the example case, this value is several times lower than the true one.

C

Experiment

4. Measurement Set-up

4.1. Power semiconductor device curve tracer

4.1.a. General description

Measurements are carried out with the Tektronix 576 curve tracer. Fig. 3 presents a simplified diagram of this device, while Fig. 4 illustrates its operating principle. Both figures correspond to a configuration used throughout a large part of this exercise, appropriate for measuring an output characteristic of a BJT with its base controlled by a current generator. There are only slight modifications in the case of a MOSFET or an IGBT:

- the step generator becomes a voltage pulse generator (u_{GS} or u_{GE} as appropriate),
- the terminal label B (base) should be replaced with G (gate),
- for a MOSFET, the label C (collector) should be replaced with D (drain), and E (emitter) should be replaced with S (source).

The operating principle of the curve tracer remains unchanged irrespectively of the type of the semiconductor device under investigation. The curve tracer generates an appropriately varying voltage between the power circuit terminals and an appropriately varying control current or voltage. This results in a quasi-static characteristic of the device under test being displayed on the screen (whose operating principle is identical to that of an analogue oscilloscope).

The basic curve tracer functions used in this exercise have been described in the brief curve tracer manual available at the laboratory stand. Before a first use of any switch or knob, it is obligatory to get acquainted with its function description. In order to facilitate operating the device, switches and knobs have been divided into four groups (A, B, C and D) according to their functions, as presented in the figure on the cover page of the additional manual. References to those groups as well as to the particular switch and knob numbers will appear further in this manual.

4.1.b. Principal (collector) circuit

The principal circuit of the device under test is supplied from a sine wave generator u_{CC} (see Fig. 3). When testing an NPN BJT, the u_{CC} waveform is full-wave rectified [see Fig. 4(a)]. As a result, the

voltage potential at the collector periodically increases up to a certain maximum of U_{CCm} and then it decreases to zero [see Fig. 9(b) where arrows indicate the trajectory of the operating point forced by the variations of the generator voltage marked in the same manner in Fig. 9(a)].

The maximum collector supply voltage U_{CCm} is set by the user with the *Max Peak Volts [A1]* switch (range selection) and the *Variable Collector Supply [A3]* knob (fine adjustment in percentage of the range). This can be expressed with the formula:

$$U_{CCm} = \textit{Variable Collector Supply} \times \textit{Max Peak Volts} \tag{4.1}$$

Caution!

Any change of the *Max Peak Volts* switch setting can only be made when the *Variable Collector Supply* knob is set to zero! Otherwise a high voltage could be abruptly applied to the collector, which might damage the device under test.

The variable loading resistor with a variable value of R_{obc} set with the *Max Peak Power [A1]* knob, is responsible for limiting power loss in the device under test ($P_C = I_C \cdot U_{CE}$). When the collector current flows, a part of the u_{CC} voltage is dropped across this resistor and consequently the maximum value of the U_{CE} voltage is lower than the maximum generator voltage U_{CCm}. The characteristic observed is thus limited by a collector circuit load line with a slope of $-1/R_L$. The power selected with the *Max Peak Power* knob corresponds to the point located in the middle of this line when the amplitude U_{CCm} is equal to the full range of *Max Peak Volts* (the *Variable Collector Supply [A3]* knob set to 100%); at other points or for lower amplitudes, the dissipated power is always smaller.

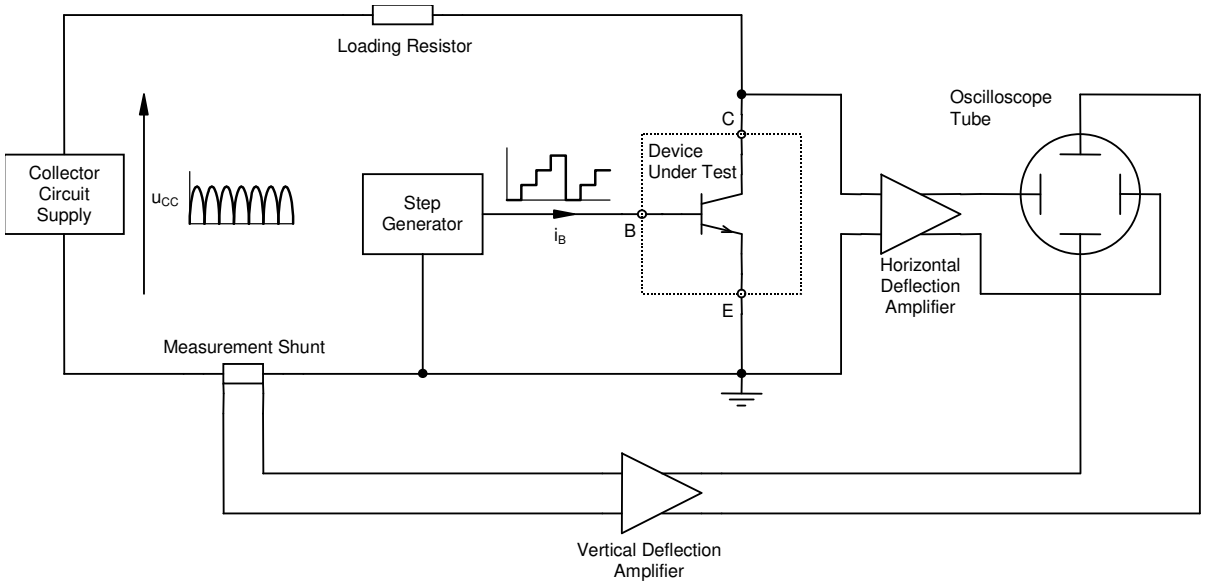


Fig. 3. Simplified diagram of the measurement circuit of the Tektronix 576 curve tracer (the configuration shown in for NPN BJT output characteristic measurement)

4.1.c. Control (base) circuit

The base of the transistor is controlled from a step wave generator which is synchronised with the sine wave collector generator. As a result, the base current takes a different value within each period of the collector voltage rectified sine wave [see Fig. 4(a)], which allows a family of characteristics to be plotted for different base current values I_B [Fig. 4(b)]. A single characteristic branch belonging to this family is plotted over each consecutive period of the u_{CC} voltage.

The number of branches (not including the zeroth branch which is always displayed) is set by the user with the *Number of Steps [B1]* switch. The base current step ΔI_B (or the height of each step) is set with the *Step/Offset Amplitude [B2]* switch.

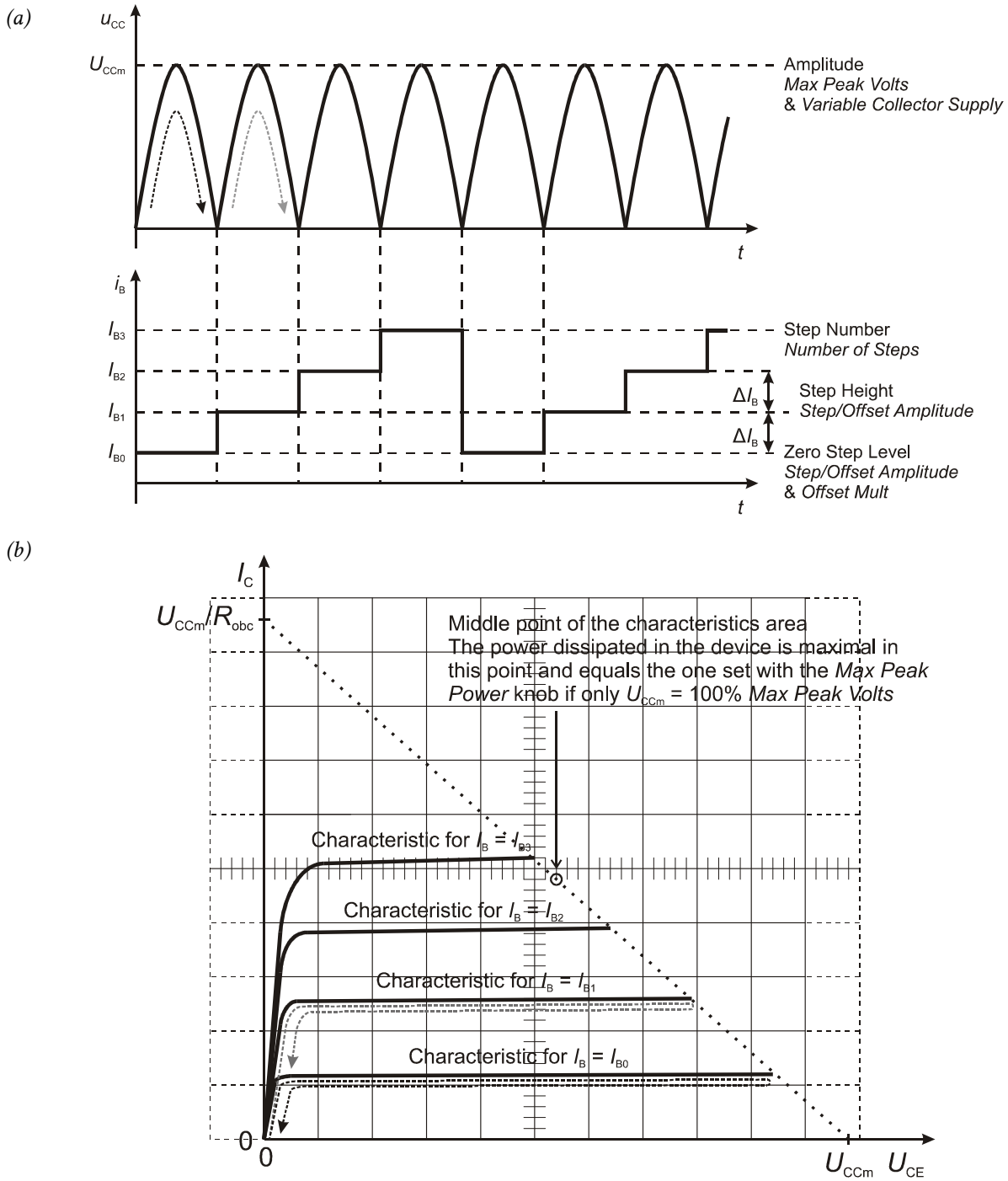


Fig. 4. Curve tracer operation during output characteristic measurements of an NPN BJT: (a) collector generator and step generator waveforms (basic waveform parameters have been marked and corresponding curve tracer switch or knob labels have been shown); (b) image generated on the screen [operating point trajectory has been marked in accordance with Fig. (a) for the two first periods of the collector generator]

The level of the zeroth step of the base current I_{B0} (corresponding to the zeroth branch of the characteristic) is:

- zero, when the *Zero* button is pressed in the *Offset [B4]* group,
- set with the *Offset Mult [B3]* knob, when the *Aid* button is pressed in the *Offset* group.

The *Offset Mult [B3]* knob is not scaled in amperes but in multiples of the step size ΔI_B (*Step/Offset Amplitude* knob), hence

$$I_{B0} = \textit{Offset Mult} \times \textit{Step/Offset Amplitude} \tag{4.2}$$

From the above equation follows a formula for the base current corresponding to the n-th branch of the characteristic:

$$\begin{aligned} I_{Bn} &= I_{B0} + n \times \textit{Step/Offset Amplitude} = \\ &= \textit{Offset Mult} \times \textit{Step/Offset Amplitude} + n \times \textit{Step/Offset Amplitude} = \\ &= (n + \textit{Offset Mult}) \times \textit{Step/Offset Amplitude} \end{aligned} \tag{4.3}$$

If the *Zero* button is pressed in the *Offset [B4]* group, then *Offset Mult* = 0 irrespectively of the actual setting of the respective knob.

4.1.d. Oscilloscope circuit

The display mechanism of the resulting characteristic image is identical to that of a classical analogue oscilloscope. The collector-emitter voltage U_{CE} is input to the horizontal deflection amplifier of the oscilloscope tube whose gain is set with the *Horizontal Volts/Div [C7]* knob. On the other hand, the voltage across the measurement shunt, which is proportional to the collector current I_C, is input to the vertical deflection amplifier whose gain is set with the *Vertical Current/Div [C1]* knob.

As a result of the coordinated action of the collector power supply, the step function generator and the oscilloscope circuit, an image of a family of output characteristics $I_C = f(U_{CE})$ of the transistor under test is plotted as shown in Fig. 4(b).

4.2. Recording results with a digital camera

4.2.a. Taking pictures

At each point of the exercise where you are required to record an observed characteristic, a picture should be taken of the curve tracer screen including the gain settings displayed on its right. This is done using a digital photo camera. At the end of the laboratory session, all pictures taken should be copied to the team's account and erased from the camera.

In order to avoid blurry images, they have to be taken using a tripod and the self-timer function of the camera. This function is turned on by pushing the ◀ button, selecting *On* with the ▼ button and accepting with the ↵ button. The self-timer automatically turns off after each picture is taken.

In order to obtain sharp images, one needs to first press the shutter button half way and wait for the camera to set the focus, which is indicated by the "AF" label with a green dot in the upper part of the display. Only then the shutter button can be pressed all the way.

The quality of the image taken can be checked by switching to the image preview mode with the ▶ button. The *W/L* button (magnifying glass) zooms the image displayed in and out.

4.2.b. Preparing for image acquisition

Before taking a first picture, it is necessary to:

1. Mount the camera on the tripod.
2. Turn on the camera.
3. Set the image resolution to 1024×768: change the operating mode to the on symbolised with a green camera, press the *MENU* button, select *Image mode* with the ▲▼ buttons and accept with the ↵ button, select *PC screen* (1024), accept, turn off the menu with the *MENU* button.
4. Turn on date imprint: set the mode knob to the *SETUP* position, select *Date Imprint* with the ▲▼ buttons, accept by pressing the ▶ button, select *Date and time*, accept with the ↵ button, return to the main menu with the ◀ button.
5. Select the *Sunset* program: set the mode knob to the *SCENE* position, press the *MENU* button, select the *Sunset* option with the ▲▼◀▶ buttons, accept with the ↵ button.
6. Turn off the flash: press the ▲ button, select the crossed out flash symbol with the ▲▼ buttons and accept with the ↵ button.

4.2.c. Image transfer to a computer

In order to download images to a computer, it is necessary to:

1. Connect the camera to a USB port of the computer and wait for the successful device installation message box to appear.
2. Copy your images from the DCIM\xxxNIKON folder on the camera to an appropriate folder on your team's account.
3. Disconnect the camera from the PC.
4. Delete the images from the camera: press the ▶ button, then *MENU*, select *Delete*, press ▶, select *Erase all images*, press ▶, select *Yes*, accept with ↵, press ▶ again.

5. Measurements

5.1. Preparing the measurement set-up

Devices to be investigated

The power transistors to be investigated are listed in Table 1. It can be noticed that they have been selected so that their ratings are very similar. Detailed data for these devices can be found in their respective data sheets appended to this laboratory manual.

Table 1. Transistors investigated in the present exercise and their principal ratings

Symbol	Transistor Type	Rated Principal Current (for a case temperature of 25 °C)		Rated Principal Voltage		Maximum Control Current or Voltage	
BU1508AX	Single BJT	I_C	8.0 A	U_{CEO}	700 V	I_B	4 A
BU808DFI	Darlington BJT	I_C	8.0 A	U_{CEO}	700 V	I_B	3 A
IRFB9N60A	MOSFET	I_D	9.2 A	U_{DSS}	600 V	U_{GS}	30 V
IRG4BC10K	IGBT	I_C	9.0 A	U_{CES}	600 V	U_{GE}	20 V

Components under test are inserted in the test circuit by mounting them in an additional adapter.

When inserting the components, the following rules must be strictly obeyed.

1. The adapter is permanently installed in the right-hand side mounting sockets of the curve tracer and must not be removed.
2. Components should be mounted so that their terminal arrangement is in accordance with the adapter labelling. The terminal arrangement for each transistor is shown in a figure found in its datasheet.
3. Component leads must not be bent.
4. During measurements, irrespectively of the voltage presently applied in the circuit, the protective cover must be closed over the device mounting connectors.
5. Field-effect transistors are sensitive to electrostatic discharge that may cause gate breakdown and thus their permanent damage. Consequently, the following **security measures must be taken**:
   - components presently not under test should be kept in an antistatic bag;

- before grabbing a component, it is necessary to remove any electrostatic charge that may be accumulated on the body, e.g. by touching the ground connector of an oscilloscope;
- a component should be held by its metal base, not by its leads.

Preliminary actions

1. Before the curve tracer is switched on:
   - make sure that in the right-hand side component mounting sockets, a green adapter has been inserted with a blue triple terminal block for component mounting;
   - if wires are led out from under the security cover on its left-hand side to an external terminal block, insert their plugs in the two lowest left-hand side sockets (labelled as E).
2. Prepare the curve tracer for use according to the guidelines listed in the operating manual (the "Setting up the curve tracer for work" box).

   While waiting for the CRT tube to warm up (the light spot to appear) one can proceed with step 3.

3. Verify if the camera settings are in accordance with those given in Section 4.2.b; make appropriate adjustments if necessary.
4. Calibrate the spot position on the curve tracer's screen:
   (a) press and hold *Zero [C6]*;
   (b) if the spot is not located precisely in the bottom left corner of the graticule (ignoring dashed lines), adjust its position with the light-grey knobs ↕ *Position [C2]* and ↔ *Position [C3]* while keeping the *Zero* button pressed;
   (c) press *Cal [C6]* and check that the spot has moved by 10 divisions right and 10 divisions upwards.
5. Turn on the normal mode of characteristic tracing: *Mode [A5] = Norm*.

Warning! At the end of the laboratory session, irrespective of how many of the measurements have been actually carried out, it is obligatory to carry out the actions listed in Section 5.4.

5.2. Output characteristics of junction transistors

Preparing the measurement set-up

When executing the following step, it is absolutely obligatory to keep all the safety measures listed in Section 5.1!

1. Identify the single BJT listed in Table 1 (an item without any additional components attached). Using its datasheet, determine its terminal arrangement (C, B, E). Plug the transistor into the adapter's terminal block, respecting its terminal labelling and tighten all its three mounting screws.
2. On the curve tracer, set:
   - the common emitter configuration with base drive from the step generator: set the *terminal connection switch [D1]* to the *Step Gen* position within the *Emitter Grounded* range (exactly this setting, not any other),
   - a collector polarity with respect to the common terminal selected above (the emitter) as appropriate for achieving the forward bias of an NPN transistor: *Polarity [A4]* = appropriate setting + (positive) or – (negative).
   - a power limit of 2.2 W: *Max Peak Power [A1] = 2.2*,
   - the current axis scale I_C (Y) to 10 mA/div: *Vertical Current/Div [C1] = Collector (not Emitter) 10 mA*,
   - the voltage axis scale U_{CE} (X) to 0.1 V/div: *Horizontal Volts/Div [C7] = Collector (not Base) .1 V (not 1)*,
   - the number of branches of the characteristic (the zeroth branch not counted) to 1: *Number of Steps [B1] = 1.*

   Also make sure that the minimum step generator current step ΔI_B of 0.05 μA is set: *Step/Offset Amplitude [B2] = .05 μA* (not any other unit, i.e. not mA or V!)

   Before proceeding with the next step, component connection and curve tracer settings must be obligatorily checked by the teacher!

3. Bias the element under test:
   (a) turn the *Variable Collector Supply [A3]* knob until a 10-division long section is displayed on the screen (which is the full graticule width, dashed lines ignored);

   According to the description in the curve tracer manual, the *Variable Collector Supply* knob is scaled in percentage of the value set with the *Max Peak Volts [A1]* knob. It only allows coarse adjustment of the collector supply voltage amplitude to be made. The precise value must be controlled on the screen.

   If at any time while carrying out the exercise, curves observed on the screen become doubled in the form of loops (instead of single lines), this may be caused by an ambiguous position of the *Display Invert [C5]* or the *Zero [C6]* button. When either button is slightly pushed and released, it should be put into a fully released position and bring the correct curve shapes back.

   The above situation may also have another cause, which cannot be completely eliminated. It is the presence of parasitic inductances which cause the operating point trajectory to be different while the voltage across the device terminals increases and while it decreases.

   (b) turn on the step generator by pressing the *On* button in the *Step Family [B8]* group;
   (c) switch *Left-Off-Right [D2]* to *Right.*

   If instead of a single, horizontal section at the bottom of the screen (according to the remark above, a slight hysteresis is admissible) anything else is observed, immediately

disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher to re-check the measurement set-up.

Single BJT

4. Make the curve tracer display a first branch of the output characteristic:
   (a) with the *Setup/Offset Amplitude [B2]* knob, increase the base current step ΔI_B until the first branch is raised above the X-axis;

   If the characteristic still has not detached from the zeroth one even at the maximum step size ΔI_B = 200 mA (a single horizontal line is displayed at the bottom of the screen), disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher to re-check the measurement set-up.

   (b) increase the Y-axis graticule constant so that collector currents of up to 4 A may be optimally observed on the screen (i.e. in a maximum zoom without the characteristic extending beyond the screen; the word „.may" just means enabling the observation, not that such currents should now be seen on the screen): *Vertical Current/Div [C1]* = appropriate *Collector* setting;
   (c) with the *Step/Offset Amplitude [B2]* knob, set the base current step to ΔI_B = 200 mA;
   (d) turn the *Variable Collector Supply [A3]* knob until a 10-division long section of the zeroth branch is displayed back on the screen.
5. Display an entire family of output characteristics:
   (a) in order not to overheat the transistor, turn off the step generator: press *Step Family [B8] / Off*;

   As a result of executing the above sub-step, only the zeroth branch should remain on the screen. If this has not happened (a fragment of the first branch is also seen near the origin of the coordinate system), ask the teacher for help.

   (b) increase the maximum power dissipated in the transistor to 50 W: *Max Peak Power [A1] = 50*;
   (c) change the number of branches to 10 (the zeroth branch not counted): *Number of Steps [B1] = 10*;

   Each time the following sub-step is executed, a family of characteristics should briefly appear on the screen, after which only the zeroth branch should remain. If this does not happen, immediately disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher for help.

   (d) press the *Single* button in the *Step Family [B8]* group; a fragment of an 11-branch family of output characteristics for the transistor under test, $I_C = f(U_{CE}, I_B)$, should briefly appear on the screen, i.e.:
      - a zeroth branch overlapping with the U_{CE} (X) axis as the *Zero* button has been pressed in the *Offset [B4]* group,
      - fragments of higher branches, most of them overlapping each other under current settings as well as cut on the right-hand and the top sides;

   If the *Single* button is pressed too frequently, this may cause the transistor to overheat as it is not efficiently cooled. This button can be pressed at most three times in sequence, after which a break of at least five seconds must follow.

   (e) check (while pressing *Single [B8]*) whether the highest branch crosses the 4 A current level in the saturation region (see Fig. 5), but does not exceed 5 A; increase or decrease the collector supply amplitude appropriately (*Variable Collector Supply [A3]* knob) if needed;

   if the above conditions cannot be met, ask the teacher to check settings.

6. Record an image of the characteristic according to the procedure given below which assures that the transistor—which is not cooled efficiently—is not overheated due to an excessive display time of the characteristic:
   (a) disconnect the power supply from the tested element by switching *Left-Off-Right [D2]* to *Off*;
   (b) turn on the step generator by pressing the *On* button in the *Step Family [B8]* group;
   (c) prepare to taking the picture by turning on the self-timer (see Section 4.2.a);

   Pictures should always be taken so that they capture not only the screen but also the settings displayed on its right-hand side ("to display" means to show on a screen, not point with a knob towards labels placed on a casing).

   (d) press the camera shutter, without supplying the component under test for now, but watching the count-down on the camera screen, only …
   (e) … when the digit 1 is displayed on the camera's screen, supply the device under test by switching *Left-Off-Right [D2]* to *Right* …
   (f) … and immediately after the shutter sound is heard, switch *Left-Off-Right* back to *Off*;
   (g) verify the quality of the image taken (see Section 4.2.a):
   - whether lines are not too blurry; if necessary, take a picture once again making sure that the camera is stable and waiting for the focus to be set (see Section 4.2.a);
   - whether settings displayed right of the screen are visible; if not, take a picture once again after re-composing the frame;
   - whether the solid frame of the graticule is visible along the perimeter of the screen; if not, adjust the graticule illumination with the *Graticule Illum* knob (top left corner of the A group) and take a picture once again;
   - whether a correct date has been imprinted in the bottom right corner of the picture, otherwise your results will be considered as cheated.

While carrying out the next step, take safety measures listed in Section 5.1!

7. Place the component tested back in the antistatic bag.

Once the curve tracer has been switched on, it should not be switched off to make switch-overs or to replace components. However, one should always ensure that the *Left-Off-Right [D2]* switch is in its *Off* position.

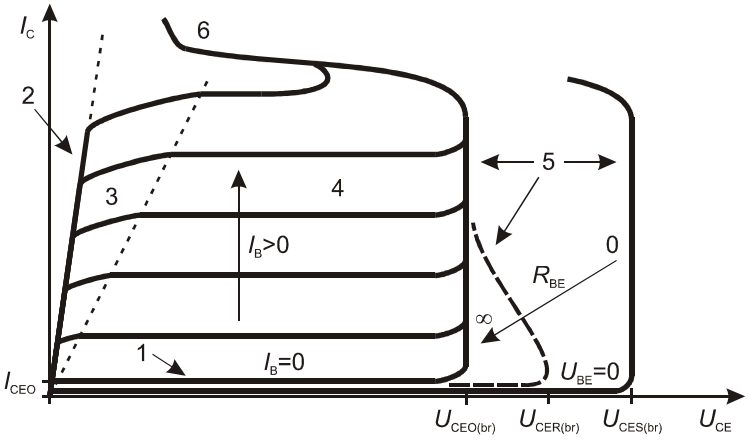


Fig. 5. Static output characteristics of a power BJT with operating regions marked: 1 blocking, 2 saturation, 3 quasi-saturation, 4 active, 5 avalanche breakdown, 6 thermal breakdown

Darlington BJT

8. * Identify the Darlington BJT listed in Table 1. Using its datasheet, determine its terminal arrangement (C, B, E). Plug the transistor into the adapter's terminal block, respecting its terminal labelling and tighten all its three mounting screws.
9. * On the curve tracer, set:
   - a power limit of 2.2 W: *Max Peak Power [A1] = 2.2*,
   - the voltage axis scale U_{CE} (X) to 0.5 V/div: *Horizontal Volts/Div [C7] = Collector .5 V*,
   - a step generator current step ΔI_B = 5 mA: *Step/Offset Amplitude [B2] = 5 mA*.

   Before proceeding with the next step, component connection and curve tracer settings must be obligatorily checked by the teacher!

10. * Display a family of output characteristics:
    (a) turn the *Variable Collector Supply [A3]* knob until a 10-division long section is displayed on the screen (which is the full graticule width, dashed lines ignored);
    (b) switch *Left-Off-Right [D2]* to *Right*;

    a fragment of an 11-branch family of output characteristics for the transistor under test, $I_C = f(U_{CE}, I_B)$, should appear on the screen, i.e.:
    - a zeroth branch overlapping with the U_{CE} (X) axis as the *Zero* button has been pressed in the *Offset [B4]* group,
    - short lower fragments of higher branches, most of them overlapping each other under current settings;

    If anything else is observed instead of the picture described above, immediately disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher to re-check the measurement set-up.

    (c) in order not to overheat the transistor, turn off the step generator: press *Step Family [B8] / Off*;

    As a result of executing the above sub-step, only the zeroth branch should remain on the screen. If this has not happened (the first branch is also seen), follow the teacher's guidelines.

    (d) increase the maximum power dissipated in the transistor to 50 W: *Max Peak Power [A1] = 50*;

    Each time the following sub-step is executed, a family of characteristics should briefly appear on the screen, after which only the zeroth branch should remain. If this does not happen, immediately disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and follow the teacher's guidelines.

    (e) while pressing *Single [B8]*, check whether the highest branch crosses the 4 A current level in the saturation region (see Fig. 5), but does not exceed 5 A; increase or decrease the collector supply amplitude appropriately (*Variable Collector Supply [A3]* knob) if needed.

    If the above conditions cannot be met, disconnect the supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher for help.

    (f) while pressing *Single [B8]*, increase the collector supply amplitude (*Variable Collector Supply [A3]* knob) so that at least three branches (apart from the zeroth one) cross the horizontal coordinate of 5 V.
11. * Record the characteristic image by repeating step 6.
12. * Taking safety measures, place the element tested back in the antistatic bag.

5.3. Output characteristics of field-effect transistors

MOSFET

When executing the following step, the safety measures listed in Section 5.1 should be taken!

1. Identify the MOSFET listed in Table 1. Using its datasheet, determine its terminal arrangement (D, G, S). Plug the transistor into the adapter's terminal block, respecting its terminal labelling and tighten all its three mounting screws.
2. On the curve tracer, set:
   - a drain polarity with respect to the common terminal selected in step 5.2/2 (in the case of a MOSFET, the source) appropriate for achieving the forward bias of an N-channel MOSFET (see Fig. 6 if in doubt): *Polarity [A4]* = appropriate setting + (positive) or – (negative),
   - a power limit of 2.2 W: *Max Peak Power [A1] = 2.2*,
   - the voltage axis scale U_{DS} (X) to 1 V/div: *Horizontal Volts/Div [C7] = Collector 1 V*.
3. Configure the step generator:
   (a) set the voltage step of the step generator ΔU_{GS} to 0.5 V: *Step/Offset Amplitude [B2] = .5 V* (not any other unit, i.e., not µA or mA!)

   An incorrect setting of the above parameter may cause the transistor to be damaged!

   (b) set the zeroth step level U_{GS0} to 3.5 V: the *Offset Mult [B3]* knob to a position corresponding to the quotient of $U_{GS0}/\Delta U_{GS}$;

   The *Offset Mult* knob is an accurate and delicate mechanical object. Use it with caution and without exerting excessive force. If it does not move or is resistant, it should be unlocked using a small lever on its side.

   The *Offset Mult* knob setting is read as follows: the integer part is indicated above the black vertical mark, the tenth parts are indicated below this mark. Since the *Number of Steps* setting is always an integer number in the present exercise, zero should be found below the mark after the adjustment is completed.

   (c) activate the *Offset Mult* knob: push *Aid* in the *Offset [B4]* group;
   (d) set the gate current I_G limit to 500 mA: *Current Limit [light B1] = 500 mA*.

Before proceeding with the next step, component connection and curve tracer settings must be obligatorily checked by the teacher!

4. Display a family of output characteristics:
   (a) turn the *Variable Collector Supply [A3]* knob until a 10-division long section is displayed on the screen (which is the full graticule width, dashed lines ignored);
   (b) switch *Left-Off-Right [D2]* to *Right*;

   a fragment of an 11-branch family of output characteristics for the transistor under test, $I_D = f(U_{DS}, U_{GS})$, should appear on the screen, i.e.:
   - a zeroth branch overlapping with the U_{DS} (X) axis,
   - short lower fragments of higher branches, most of them overlapping each other under current settings;

   If anything else is observed instead of the picture described above, immediately disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher to re-check the measurement set-up.

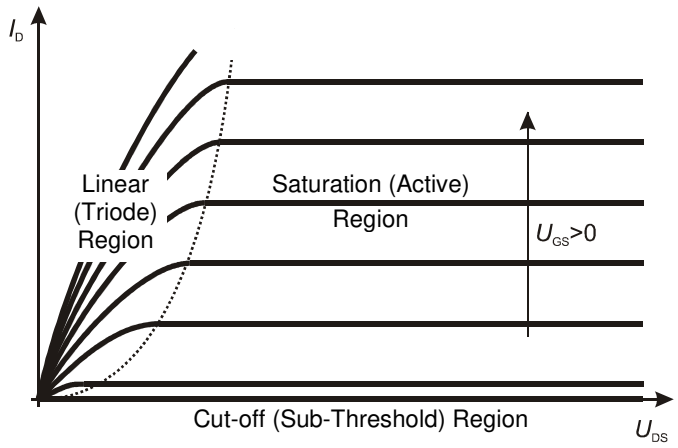


Fig. 6. Static forward output characteristic of an N-channel power MOSFET with operating regions labelled

(c) in order not to overheat the transistor, turn off the step generator: press *Step Family [B8] / Off*;

As a result of executing the above sub-step, only the zeroth branch should remain on the screen. If this has not happened (the first branch is also seen), follow the teacher's guidelines.

(d) increase the maximum power dissipated in the transistor to 50 W: *Max Peak Power [A1] = 50*;

Each time the <u>following</u> sub-step is executed, a family of characteristics should briefly appear on the screen, after which only the zeroth branch should remain. If this does not happen, immediately disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and follow the teacher's guidelines.

(e) while pressing *Single [B8]*, check whether the highest branch crosses the 4 A current level in the <u>linear</u>, i.e. triode, region (according to the terminology applicable to the MOSFET; cf. Fig. 6 if in doubt) but does not exceed 5 A; increase or decrease the collector supply amplitude appropriately (*Variable Collector Supply [A3]* knob) if needed;

If the above conditions cannot be met, disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher for help.

(f) <u>imperatively</u> write down the present setting of the *Offset Mult [B3]* knob.

5. Record the characteristic image by repeating step 5.2/6.
6. Taking safety measures, place the element tested back in the antistatic bag.

IGBT

7. While taking safety measures, identify the IGBT listed in Table 1. Using its datasheet, determine its terminal arrangement (C, G, E). Plug the transistor into the adapter's terminal block, respecting its terminal labelling and tighten <u>all its three</u> mounting screws.
8. On the curve tracer, set:
   - a collector polarity with respect to the common terminal selected in step 5.2/2 appropriate for achieving the forward bias of an N-channel IGBT (see Fig. 7 if in doubt): *Polarity [A4]* = appropriate setting + (positive) or – (negative),
   - a power limit of 2.2 W: *Max Peak Power [A1] = 2.2*,
   - the voltage axis scale U_{DS} (X) to 0.5 V/div: *Horizontal Volts/Div [C7]* = <u>*Collector .5 V*</u>

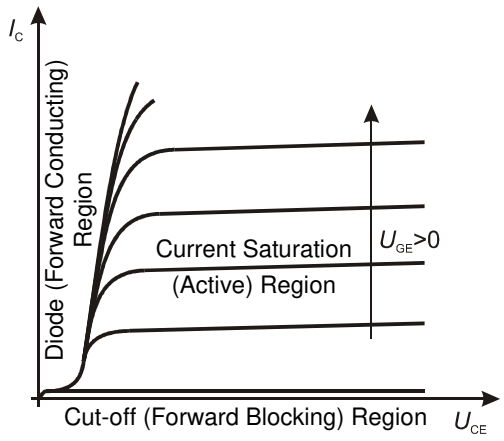


Fig. 7. Static forward output characteristic of an N-channel IGBT with operating regions labelled

9. Configure the step generator by setting:
   - the voltage step of the step generator ΔU_{GE} to 1 V: *Step/Offset Amplitude [B2] = 1 V* (not any other unit),
   - the zeroth step level U_{GE0} to 6.0 V: the *Offset Mult [B3]* knob to a position corresponding to the quotient of $U_{GE0}/\Delta U_{GE}$.

   Before proceeding with the next step, component connection and curve tracer settings must be obligatorily checked by the teacher!

10. Display a family of output characteristics:
    (a) turn the *Variable Collector Supply [A3]* knob until a 10-division long section is displayed on the screen (which is the full graticule width, dashed lines ignored);
    (b) switch *Left-Off-Right [D2]* to *Right*;

    a fragment of an 11-branch family of output characteristics for the transistor under test, $I_C = f(U_{CE}, U_{GE})$, should appear on the screen, i.e.:
    - a zeroth branch overlapping with the U_{CE} (X) axis,
    - short lower fragments of higher branches, most of them overlapping each other under current settings;

    If anything else is observed instead of the picture described above, immediately disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher to re-check the measurement set-up.

    (c) in order not to overheat the transistor, turn off the step generator: press *Step Family [B8] / Off*;

    As a result of executing the above sub-step, only the zeroth branch should remain on the screen. If this has not happened (the first branch is also seen), follow the teacher's guidelines.

    (d) increase the maximum power dissipated in the transistor to 50 W: *Max Peak Power [A1] = 50*;

    Each time the following sub-step is executed, a family of characteristics should briefly appear on the screen, after which only the zeroth branch should remain. If this does not happen, immediately disconnect the supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and follow the teacher's guidelines.

(e) while pressing *Single [B8]*, check whether the highest branch crosses the 4 A current level in the forward conducting, i.e. diode, region (according to the terminology applicable to the IGBT; cf. Fig. 7 if in doubt) but does not exceed 5 A; increase or decrease the collector supply amplitude appropriately (*Variable Collector Supply [A3]* knob) if needed;

If the above conditions cannot be met, disconnect the power supply from the device under test by switching *Left-Off-Right [D2]* to *Off* and ask the teacher for help.

(f) imperatively write down the present setting of the *Offset Mult [B3]* knob.

11. Record the characteristic image by repeating step 5.2/6.
12. Taking safety measures, place the element tested back in the antistatic bag.

5.4. Concluding measurements

1. Make sure that the power supply is disconnected from the device under test: *Left-Off-Right [D2]* is set to *Off*.
2. Bring curve traces settings back to safe ones:
   - zero collector voltage: turn *Variable Collector Supply [A3]* to its extreme anticlockwise position,
   - power limit of 0.1 W: *Max Peak Power [A1]* = 0.1,
   - minimum current step ΔI_B: *Step/Offset Amplitude [B2] = .05 μA*,
   - current limit I_B to 20 mA: *Current Limit [light B1] = 20 mA*,
   - step generator turned off: push *Step Family [B8] / Off*,
   - Y-axis scale of 10 mA/div: *Vertical Current/Div [C1] = Collector 10 mA*,
   - *Offset Mult* knob de-activated: push *Offset [B4] / Zero*.
3. Switch the curve tracer off: switch *Power [A2]* to *Off*.
4. Copy the pictures taken to your team's account on the computer and erase them from the camera's memory (see Section 4.2.c).

D

Results

6. Processing and Analysing Results

6.1. Static forward characteristics

1. In a static output characteristic image for each of the three devices tested (* the Darlington BJT excluded), mark and label all the visible operating regions(see, and; not all the possible operating regions of the investigated devices can be seen in the images recorded). Include the images so processed in the appropriate space provided in Part 1 of the report.

   Operating regions in a static output characteristics of a BJT have been shown in Fig. 5; they are also presented and described in Ref. A. An appropriate plot for a MOSFET have been shown in Fig. 6; a static output characteristic of this device is also presented in Manual 0, Ref. H, and described in Manual 3P, Ref. A. Similarly, a plot for an IGBT can be found in Fig. 7; a static output characteristic of this device is also presented in Manual 0, Ref. H, and described in Manual 4P, Ref. A.

2. Run the OOo Digitizer (Digitizer of XY chart, Digitizer wykresów) program:
   (a) download the program from the web page http://extensions.libreoffice.org/extension-center; depending on your preference, select a LibreOffice extension package (an OXT file) or a standalone application package;
   (b) to use the program as a LibreOffice extension:
   - in any LibreOffice application, select *Tools* ▸ *Extension Manager* ▸ *Add* and open the file downloaded,
   - after installation completes, close the entire LibreOffice package (all the open applications) and then, re-start Calc;

   to use the program as a standalone application:
   - unpack downloaded files in any folder,
   - for the application to run, Java Runtime Environment (JRE) has to be installed,
   - automated data transfer to LibreOffice or OpenOffice.org can be enabled by selecting *Settings* ▸ *L/O Office directory* from the menu and pointing to the folder containing the file *calc.exe*;

(c) launch the program according to the selected option:
- under LibreOffice Calc, from the list under the menu item *Tools* ▸ *Add-Ons*,
- or as a standalone application, by running the *OOoD_*.jar* file found in the application's main folder.

3. From the output characteristic of the single BJT, read out a set of points (U_{on}; I_o) located in the saturation region:
   (a) in OOo Digitizer, open the recorded image of a static output characteristic of the transistor indicated by going to the *Image* tab and selecting *Image* ▸ *Load* from the menu; it is best to process an image in its original scale, but if it does not fit the screen, it can be zoomed out by checking *Zoom*, clicking the edit box beside and entering an appropriate zoom of less than 1;
   (b) configure the coordinate axes:
   - go to the *Axis* tab,
   - make both axes originate at a common point by checking the *[X-axis P1]=[Y-axis P1]* option,
   - select the origin point of the X-axis (*X-axis* / *P1*), then click the graph at the point of (*X*; *Y*) = (0 div; 0 div) of the graticule (dashed lines not counted, cf. Fig. 8), fine-tuning its position with the *Tune point* arrows ← ↑ ↓ → if needed,
   - in the *X-axis* / *P1* / *X* field, enter the value of 0 V (skipping the unit), corresponding to the origin of the coordinate system,
   - select the end point of the X-axis (*X-axis* / *P2*), then click at the point of (*X*; *Y*) = (10 div; 0 div), fine-tuning its position with the arrows if needed,
   - in the *X-axis* / *P2* / *X* field, enter the value of voltage that corresponds to 10 divisions of the horizontal scale, thus ten times the *Per Horiz Div* setting displayed right of the screen (it would be *2* in the case of Fig. 8),
   - in the *Y-axis* / *P1* / *Y* field, enter the value of 0 A (skipping the unit), corresponding to the origin of the coordinate system,
   - select the end point of the Y-axis (*Y-axis* / *P2*), then click at the point of (*X*; *Y*) = (0 div; 10 div), fine-tuning its position with the arrows if needed,
   - in the *Y-axis* / *P2* / *Y* field, enter the value of voltage that corresponds to 10 divisions of the vertical scale, thus ten times the *Per Vert Div* setting displayed right of the screen (it would be *10* in the case of Fig. 8);
   (c) go to the *Digitize* tab and set up the following:
   - turn on axis display by checking *Draw* ▸ *Axis* in the menu,
   - change point colour to any one that will stand out from the green lines in the image (e.g. yellow; the default colour being unfavourably green) by selecting *Draw* ▸ *Unselected points color*;
   (d) create a new data series by selecting *Series* ▸ *Add* from the menu and name it arbitrarily;
   (e) by clicking the characteristic and fine-tuning the point position with the *Tune point* arrows if needed, select fairly accurately 5 to 10 points that correspond to the transistor's operation in its saturation region with a low voltage drop (see Fig. 8), fairly uniformly distributed in the range (i.e. not outside this range) of current from 0.5 A to 4 A, including the extreme values (i.e. 0.5 A and 4 A);

   In your imagination, draw a straight line parallel to the voltage axis, located at the level of the current chosen. Then, moving left along this line, reach a branch that crosses this chosen current level in its full saturation region (not in the active or quasi-saturation one). Next, consider the low voltage drop requirement.

   The notion of a '*low* voltage drop' is obviously relative. However, characteristic branches exhibit a tendency to become closer to each other as the control quantity increases to finally form a single thick line on the screen. Assume that a voltage is 'low' when a given branch is already indistinguishable from the neighbouring one on its left (still following the horizontal line corresponding to the chosen current).

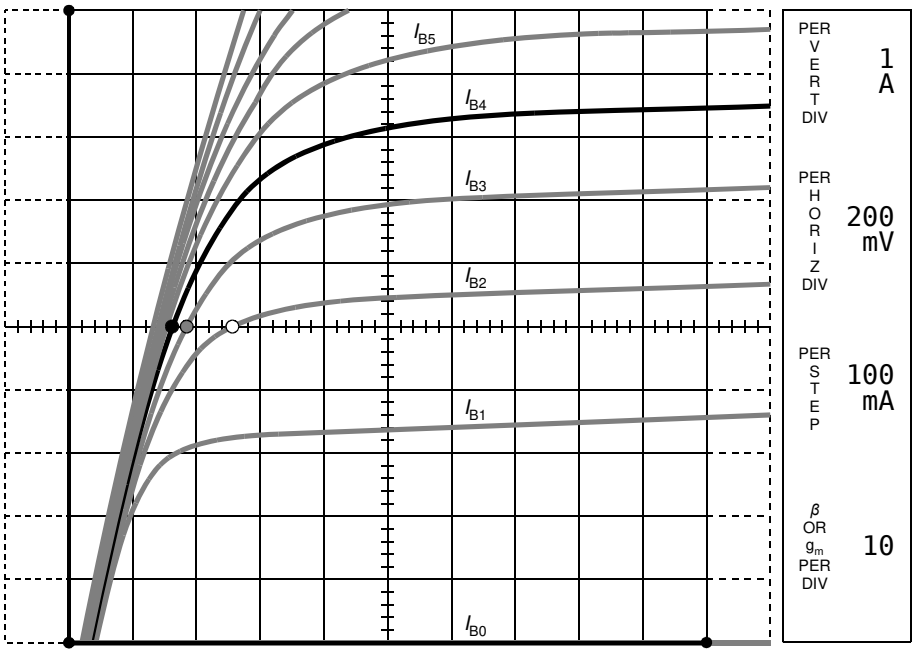


Fig. 8. Defining the coordinate system axes (lines ending with dots) and locating an operating point in the saturation region of a BJT characteristic for an example principal current coordinate $I_o = I_C = 5$ A (curves in the image are idealised and do not have any quantitative relation to those obtained in this exercise)

For example, in Fig. 8 a suitable operating point has been marked for a principal current of I_o = 5 A (corresponding to a vertical coordinate of Y = 5 div). The minimum control current value for which the principal current of 5 A is achieved, is I_{B2} (the white dot), but this happens outside of the saturation region. On the other hand, for the control current of I_{B3} (the grey dot), the voltage is relatively high as the corresponding curve lies well to the right of its neighbour curve. Only the branch for the control current of I_{B4} meets the requirements formulated above (the black dot).

(f) move the point coordinates $(X; Y) = (U_{on}; I_o)$ read out to a spreadsheet:

- if using the LibreOffice extension, select *Series* ▸ *Save in Calc* from the menu, which should cause a new worksheet to be opened where cells have been filled with the data contained in the table found in the *Points* frame in OOo Digitizer,
- in any other case, select *Series* ▸ *Save and CSV* from the menu, then open (import) the file saved in a spreadsheet,
- do not close OOo Digitizer;

In the case presented in Fig. 8, the $(U_{on}; I_o)$ coordinates of the operating point marked should be (0,32; 5) provided the coordinate system axes have been defined correctly according to that image.

(g) in the spreadsheet, label the columns X and Y as on-state voltage U_{on} and principal current I_o, respectively, adding appropriate units.

4. Complement the data read out until now with the control current I_{ctrl}:

(a) make a screenshot with the OOo Digitizer window and, using any image processing software, crop it so that to cover only the curve tracer's screen together with settings displayed in the fields on its right (cf. Fig. 8);

(b) in the image obtained, label each characteristic branch with a corresponding value (i.e. a number with a unit) of the control current I_{ctrl} (the I_B current in the case of a BJT), considering the following:

- formulae (4.3) and (4.2) should be applied,

- the generator's step ΔI_{ctrl} (ΔI_B for a BJT) is the *Step/Offset Amplitude* knob setting displayed in the *Per Step* field in the image,
- the level of the zeroth step I_{ctrl0} (I_{B0} for a BJT) results from the fact that for the BJTs, the *Offset / Zero* button was pressed or, respectively, from the *Offset Mult* setting written down (for the MOSFET and for the IGBT),
- according to the description presented in Section 4.1.c, the lowest branch corresponds to $n = 0$ (not 1);

(c) insert the characteristic image with points marked and branches labelled with control quantity values in the appropriate space provided in Part 1 of the report;

(d) based on the processed image, for each of the points (U_{on}; I_o) obtained in step 3, read out and add to the spreadsheet the control current value I_{ctrl} that corresponds to the branch where the given point belongs (with an accuracy of the generator's step, thus of the labels added).

In the case presented in Fig. 8, for the operating point marked, $I_{ctrl} = I_B = I_{B4} = 0$ mA + 4×100 mA = 400 mA, because the corresponding branch has number 4 and $I_{B0} = 0$ mA due to the *Offset / Zero* button having been pressed.

5. For each of the points (U_{on}; I_o) obtained in step 3, from the data sheet of the investigated transistor, read out a value of the control circuit voltage $U_{ctrl} = U_{BE}$ corresponding to the transistor's operation in its saturation region at each particular value of the output current I_o [the $U_{BE(sat)} = f(I_C)$ characteristic]. Add the values read out to the spreadsheet.

Thanks to the short measurement duration, it can be assumed that transistors were not heating up, hence the semiconductor temperature inside them was equal to the room temperature. Readouts of any temperature-dependent parameters should therefore be made for the junction temperature T_j of 25 °C.

6. * Repeat steps 3 to 5 for the Darlington BJT.

To enable comparisons to be made, the same principal voltage unit, the same principal current unit and the same control current or voltage unit should be applied.

7. For the MOSFET and for the IGBT:

(a) repeat step 3 with the exception that it is the linear (triode) region of the output characteristic that corresponds to a MOSFET fully on while the forward conduction (diode) region corresponds to an IGBT fully on;

(b) repeat step 4 with the exception that in the case of the above transistors:

- it is the input voltage U_{ctrl} (i.e. U_{GS} or U_{GE}, respectively) that is the control quantity,
- the *Offset Mult* knob setting was written down in step 5.3/4(f) or 10(f), respectively;

(c) for each of the control voltage values written down determined in sub-step (b), from an appropriate gate charge characteristic given in Fig. 2, in the way described in Section 3.2.d, read out the charge value $Q_{in} = Q_{G(tot)}$ supplied in the control circuit during the transistor's switching, corresponding to each particular control voltage U_{GS} or U_{GE} and (approximately) to a suitable (observed at the same operating point) principal current I_o. Add the values read out to the spreadsheet.

8. Based on the results collected in spreadsheets, for each of three (* four) transistors, calculate (in the same spreadsheet):

To enable comparisons to be made, the same units should be applied for all the transistors to each of the particular quantities being calculated.

(a) the on-state resistance

$$R_{on}(I_o) = \frac{U_{on}(I_o)}{I_o} \tag{6.1}$$

(b) average static principal circuit power loss P_{loss} (see Sub-chapter 3.1;

The above task requires specific operating conditions to be assumed. They have to be identical and reasonable for all the transistors so that reliable comparisons could be made. For the purpose of this exercise, assume the simplest case of switch-mode operation with a duty cycle of $D = 0.5$.

(c) average control power P_{ctrl} (see Sub-chapter 3.2).

In order for the results to be coherent, the previous assumption of $D = 0.5$ should be maintained. To calculate control power for charge-controlled devices, it is necessary to additionally assume a specific switching frequency f_s. The value of 10 kHz should be assumed, which is an approximate application boundary between BJTs and MOSFETs as well as an average (in the logarithmic scale) application frequency of IGBT.

9. Include the numerical results of steps 3 to 8 in appropriate tables in Part 1 of the report.

6.2. Comparative analysis of static properties

On-state voltage drop and resistance

1. Fill in Part 2 of the report.

Principal circuit static power loss

2. Fill in Part 3 of the report.

Control power consumption

3. Fill in Part 4 of the report.

Static current gain

4. For the single (* and the Darlington) BJT, calculate the static forward current gain in the common emitter configuration β_F, from its definition:
   (a) in the saturation region, for a freely chosen (from the available data) collector current value I_C (considering that the collector current is the principal one for a BJT), based on the results found in an appropriate table in Part 1 of the report;
   (b) in the quasi-saturation region, for the voltage of $U_{CE} = 1\,V$ (* or $U_{CE} = 5\,V$ for the Darlington), from an appropriate characteristic obtained in step 6.1/4, while:
      - a characteristic branch should be selected that for the U_{CE} value given above exhibits a value of I_C possibly close to the one chosen in sub-step (a),
      - the value of I_C for the point defined above should be read out from the curve tracer's screen graticule,
      - the value of I_B corresponding to the selected branch should be read out from the labels added to the graphic.
5. Place source data extracted from tables and characteristics as well as calculation results in the table found in Part 5 of the report.
6. Complete Part 5 of the report.

BJT compared to other types of power transistors

7. Fill in Part 6 of the report.

E

Information

7. Required Knowledge

7.1. Prerequisites

- Main circuit and drive circuit terminals, static output characteristics and regions of operation for power BJT, MOSFET and IGBT
  (Ref. A; Manual 3P, Ref. A; Manual 4P, Ref. A; figures in Sections 5.2 and 5.3)
- General operating principle of the curve tracer used in this exercise for the BJT output characteristic measurement case: collector supply (maximum voltage), gate generator (generator step, zeroth branch current)
  (Section 4.1)

7.2. Test scope

1. High-voltage BJT: terminals, semiconductor structure cross-section, static output characteristic; operating regions, general picture of physical phenomena (especially, junction biasing and excess free carrier extension), location in the output characteristic; the difference in static and dynamic parameters between the saturation and quasi-saturation modes
   (Ref. A, Manual 0, Ref. H, 3.1.2)
2. BJT (common-emitter) current gain: definition (formula), typical values for power transistors, effect of collector current (plot, physical origins) and of the operating region (physical origins)
   (Ref. A)
3. Classification of power transistors with respect to the control mechanism criterion and with respect to the conduction mechanism criterion, as applied to the devices investigated
   (Manual 0, Ref. H; report)
4. Principal circuit power loss and control power for the three transistor types (single BJT, MOSFET, IGBT; formulae)
   (Sections 3.1, 3.2)
5. Forward output characteristic, on-state resistance, principal circuit power loss and control power as functions of principal current for the three different transistor types (single BJT, MOSFET, IGBT) combined in a single plot (linear or logarithmic scale as in the report); relation to physical control and conduction mechanisms as well as to the control quantity
   (report; Manual 0, Ref. H)

6. Advantages and drawbacks of the different three transistor types (single BJT, MOSFET, IGBT) considered as power electronic switches, with regard to the power (principal) circuit and with regard to the control circuit; resulting potential application areas, considering different load currents; reasons for applying BJTs (see report)

8. References

[1] Benda V., Gowar J., Grant D. A.: *Power Semiconductor Devices: Theory and Applications*. Wiley, 1999. ISBN 0-471-97644-X.