Design of CMOS Circuits

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Standard cells design guidelines

All layout designs should have the form of standard cells, with the exception of ring oscillators.

1. Transistors may be always drawn in pairs: 1 PMOS at the top, 1 NMOS at the bottom. However, a higher grade can be obtained for better transistor placement.
2. Gate polysilicon should run in a straight line within the transistors and at a distance of minimum polysilicon protruding over diffusion (rule r305—see textbook). (Note: This rule results only from Microwind's limitations—it cannot extract transistor dimensions correctly otherwise. Figure 12-7 in the lecture notes shows that cell dimensions can be reduced if the gate is bent.)
3. Outside the transistors there is no restriction on the polysilicon shape. This allows cell dimensions to be reduced.
4. All the cells must have the same height. Lower and upper cell boundaries are defined by the corresponding edges of VDD and VSS buses.
5. The height of the cell should be such that all transistors and internal connections fit inside for the most complex cell. In the case of this course this will be the D flip-flop with reset and the T flip-flop. You may get some idea about the size of these cells looking at Fig. 3.
6. The width of the cell should be as low as possible so as all cell components fit inside without violating the design rules. Left and right cell boundaries are defined by the corresponding edges of VDD and VSS buses.
7. The cells can be abutted in two ways:
   (a) horizontal abutment, when cells are placed in a row; one or both cells may be mirrored horizontally;
   (b) vertical abutment, when cells are components of neighbouring rows; one of the cells must be mirrored vertically and one or both may be mirrored horizontally.

   In the case (a), the supply buses and the wells of both cells must fit perfectly at cell boundaries. The position of the supply buses and the well should be kept unchanged across the entire cell width. When minimizing cell dimensions, the well height may be decreased or increased inside the cell; this, however, requires special care so as design rules conformity is maintained at cell boundaries when two cells are abutted (rules r101, r102, r203, r204).

   In the case (b), the shape of the supply buses and the well should ensure their connection over the entire common boundary.
8. The supply buses should be drawn in metal 1. When choosing their height, take into account that they will be supplying a large number of cells.
9. Over the entire cell width, well or substrate bias contacts should be placed on the supply buses. Rightmost and leftmost contacts should be placed as close as possible to the cell boundary. Their distance to cell boundaries (left, right, and top or bottom) should ensure fulfilment of design rules when abutting cells horizontally or vertically (r202).

10. All metal paths (apart from the ones connecting the cell with other cells, including supply buses), polysilicon paths and N^+ i P^+ diffusions must be placed far enough from the left and right edges of the cell to ensure fulfilment of design rules when abutting cells horizontally (r202, r302, r502, r702).
11. The well should extend outside the supply bus for the minimum well-over-diffusion spacing (rule r203) decreased by the protrusion of supply bus metal over the rightmost and leftmost contact diffusion (rule 7).
12. Each input and each output of the cell should have a contact to metal 2. External connections in metal 2 or metal 3 will be connected here.
13. Interconnections inside the cell should be routed using mainly metal 1. If two metal tracks need to be crossed, a metal 2 bridge has to be made on one of the tracks (as short as possible, as metal 2 is intended to be used for vertical external connections); as a last resort make a metal 3 bridge. Signals that are connected to transistor gates may also be routed using polysilicon, especially when this allows to avoid additional contacts.
14. To ensure the lowest resistance, signals should be connected to drains and sources using as many contacts as possible to fit over the diffusion area; metal should run uninterrupted from the first to the last contact.
15. Polysilicon width within transistors should be equal to the optimal (i.e., minimal) channel length. Outside the transistors, starting from the minimum polysilicon protrusion over diffusion, the tracks may be widened up to 3–4 λ, which allows to reduce their resistance.

Interconnection of standard cells

The counter should be a circuit composed of appropriate number of standard cells. Specific cells should be placed so as to obtain minimum interconnection lengths and the shape of entire circuit as close to a square as possible.

Connections between input/output contacts of different standard cells should be routed over the cells with metal. Vertical connections should be realized using metal 2, whereas horizontal connections using metal 3. At short distances (comparable to contact size) it is allowed to ignore these restrictions.

Examples of correct designs

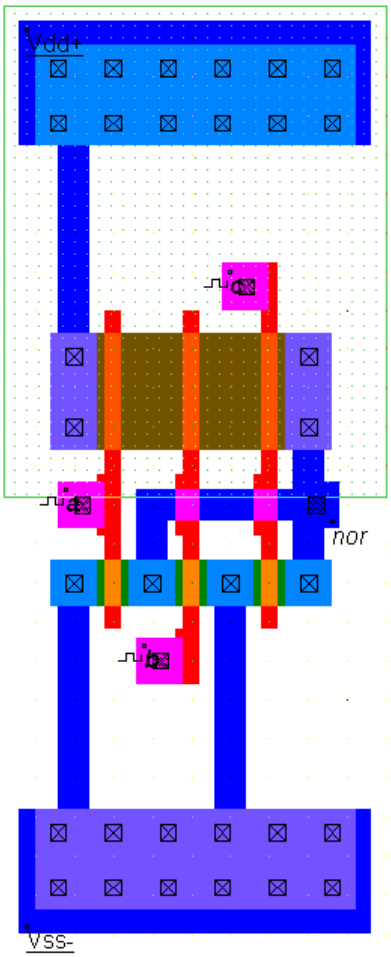

Fig. 1. Three-input NOR gate with transistors placed pairwise one over another.

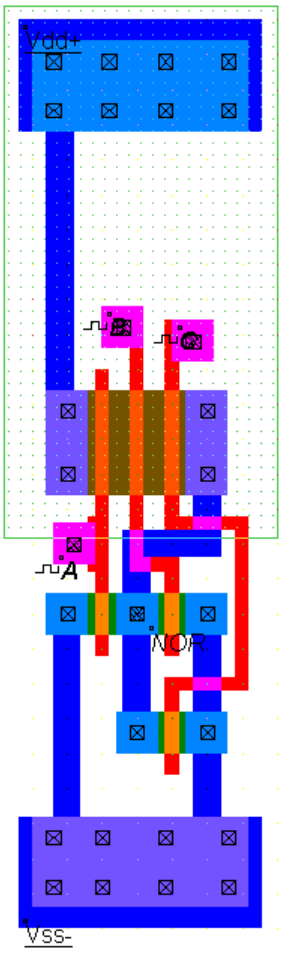

Fig. 2. Three-input NOR gate with optimized width.

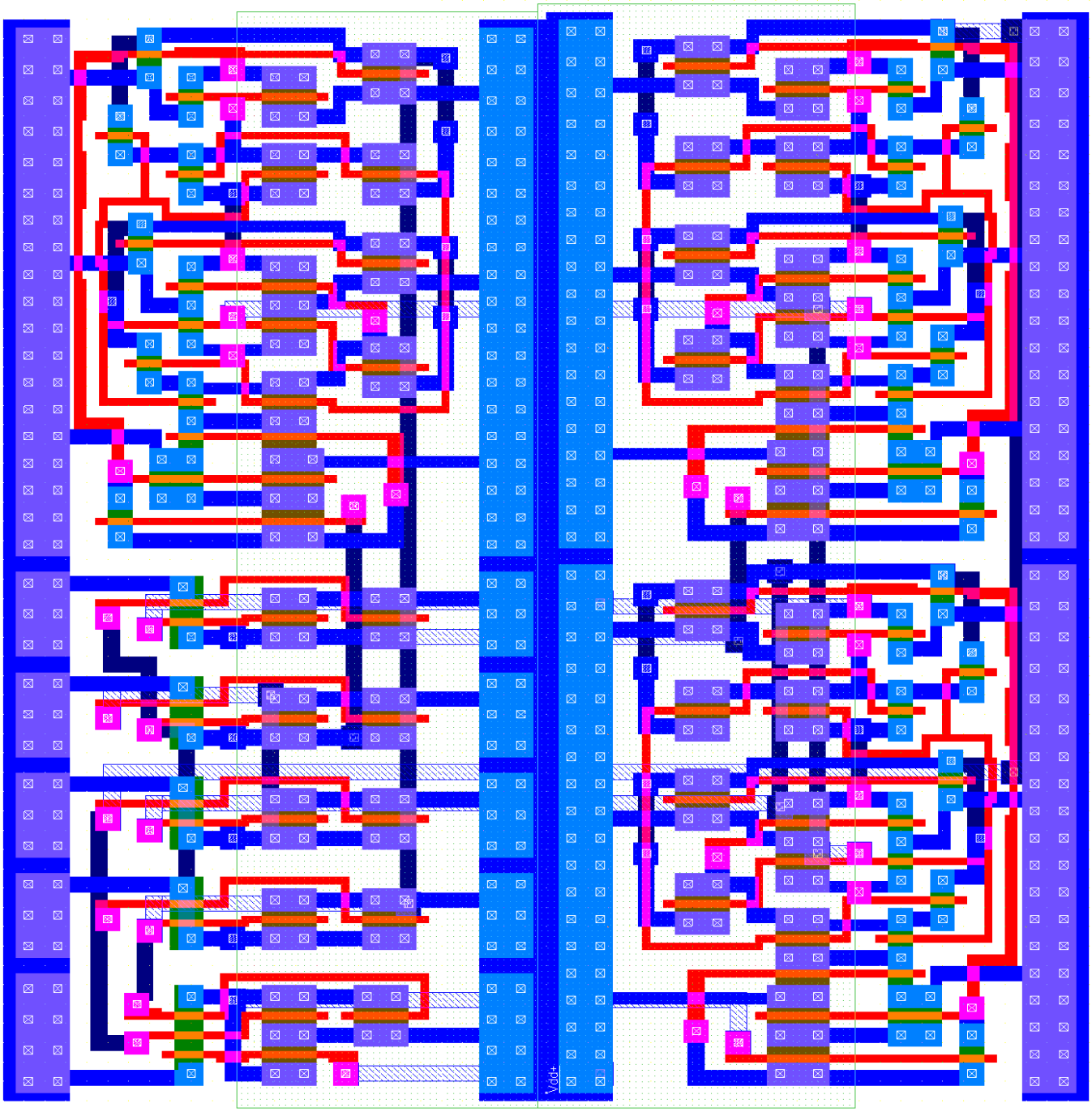

Fig. 3. Three-bit counter counting in a loop from 0 to 6, composed of standard cells (starting from top left; this page should be rotated 90 degrees clockwise): 1 three-input NAND gate, 4 two-input NAND gates, and 3 T-type flip-flops.

To be remembered when working with Microwind

- Always choose the proper technology after starting the program.
- Always decrease the simulation step by a factor of 10 at first run.
- Undo function works only for the last (one) operation.

Solutions to frequent problems in Microwind

Problem	*Possible Cause and Solution*
The inserted contact has strange dimensions.	No technology has been chosen. Choose your technology, then remove the contact and insert it again.
A waveform does not appear in the simulation window although a visible node has been placed in the circuit.	The layer on which the visible node has been placed is shorted with another one that already has a name assigned. The name may be assigned through a clock signal, another visible node, or a supply voltage (Vdd, Vss). As waveforms in the shorted points are in fact one waveform, only one of them is plotted in the simulation window (or none of them if there is short to Vdd or Vss). If this behaviour is not correct, it indicates a mistake in design.
Delay times are not displayed.	There may be several reasons. Display/Delay option is not checked. Input (“between” field) and output (“and” field) signals have not been properly chosen. The simulation step is too large. The circuit is not yet in its steady state; click More several times to reach the steady state. The delay times are too short to be measured; reduce slope steepness of the input clock and/or load the output with an inverter.
The measured delay times are different for different various periods.	The circuit has not reached its steady state yet. Click More so as delays are measured after some 10–20 switching periods. If this does not help, the simulation step may be too large and the results are too inaccurate.
Voltage waveforms have irregular form, often with short spikes.	The simulation step is too large which causes numerical errors and poor accuracy.
The delay times measured at home and in class are different.	Different technology files are used (check sizes and modification times), or simulation times are different, or clock parameters are different.
The circuit acts properly from the logic point of view but the voltage does not reach the top grid line of the plot. (Note: In some circuits this behaviour is normal.)	Check if the substrate and the wells are properly supplied. Check if the circuit is supplied from the core supply (“blue” Vdd) not the peripheral one (“red” Vdd). Check the same in all clocks.