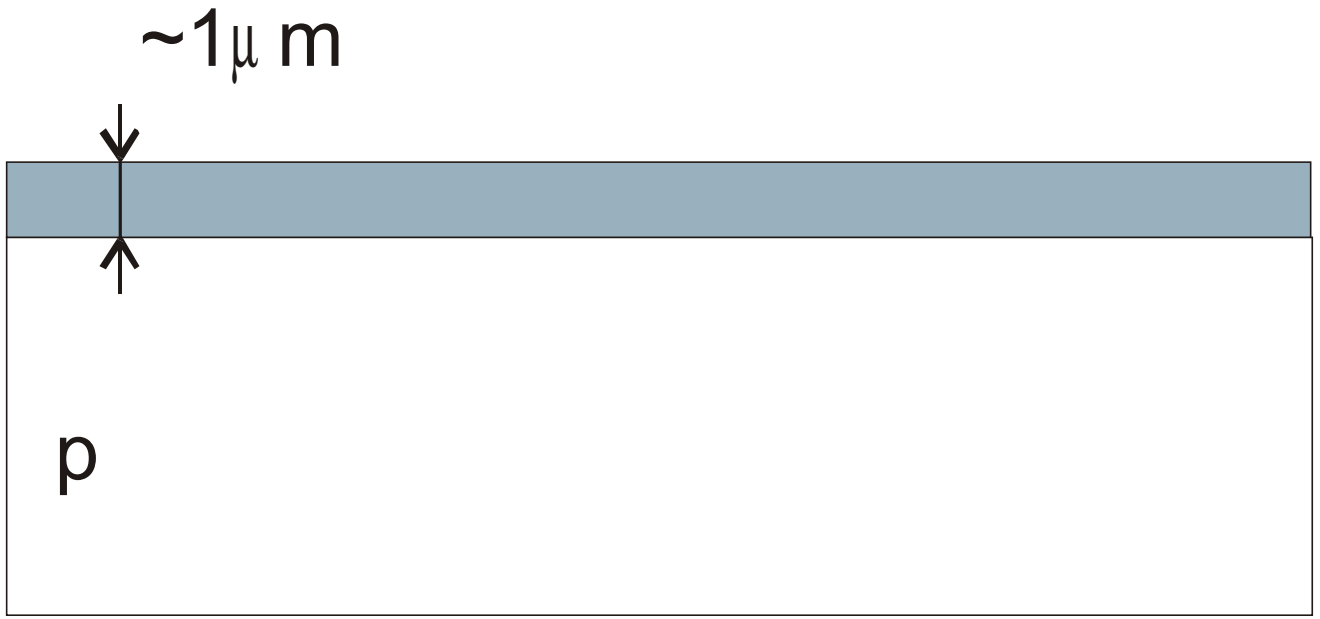
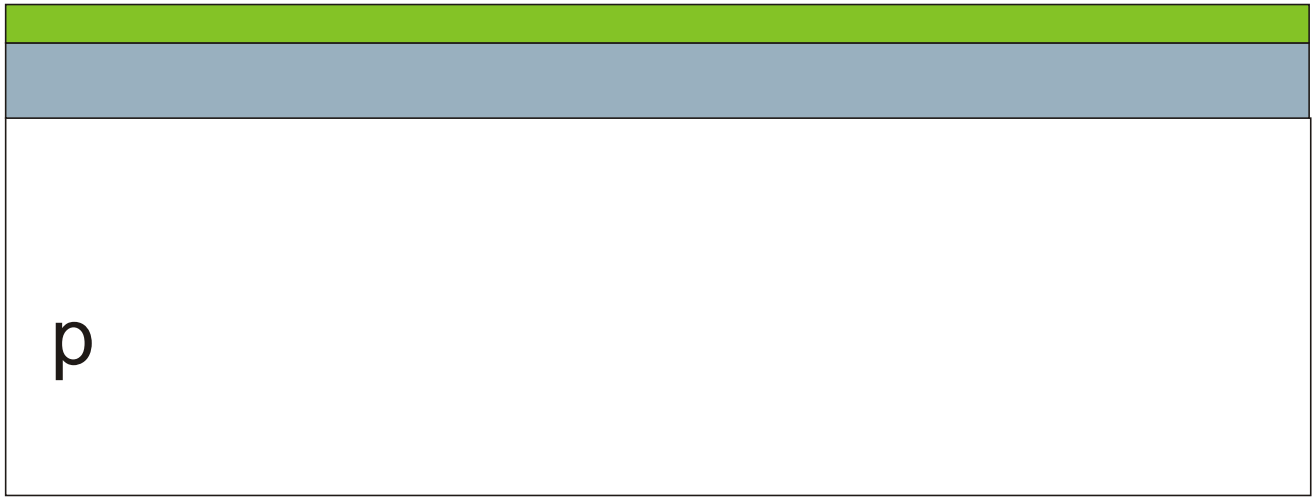
N-well CMOS Process

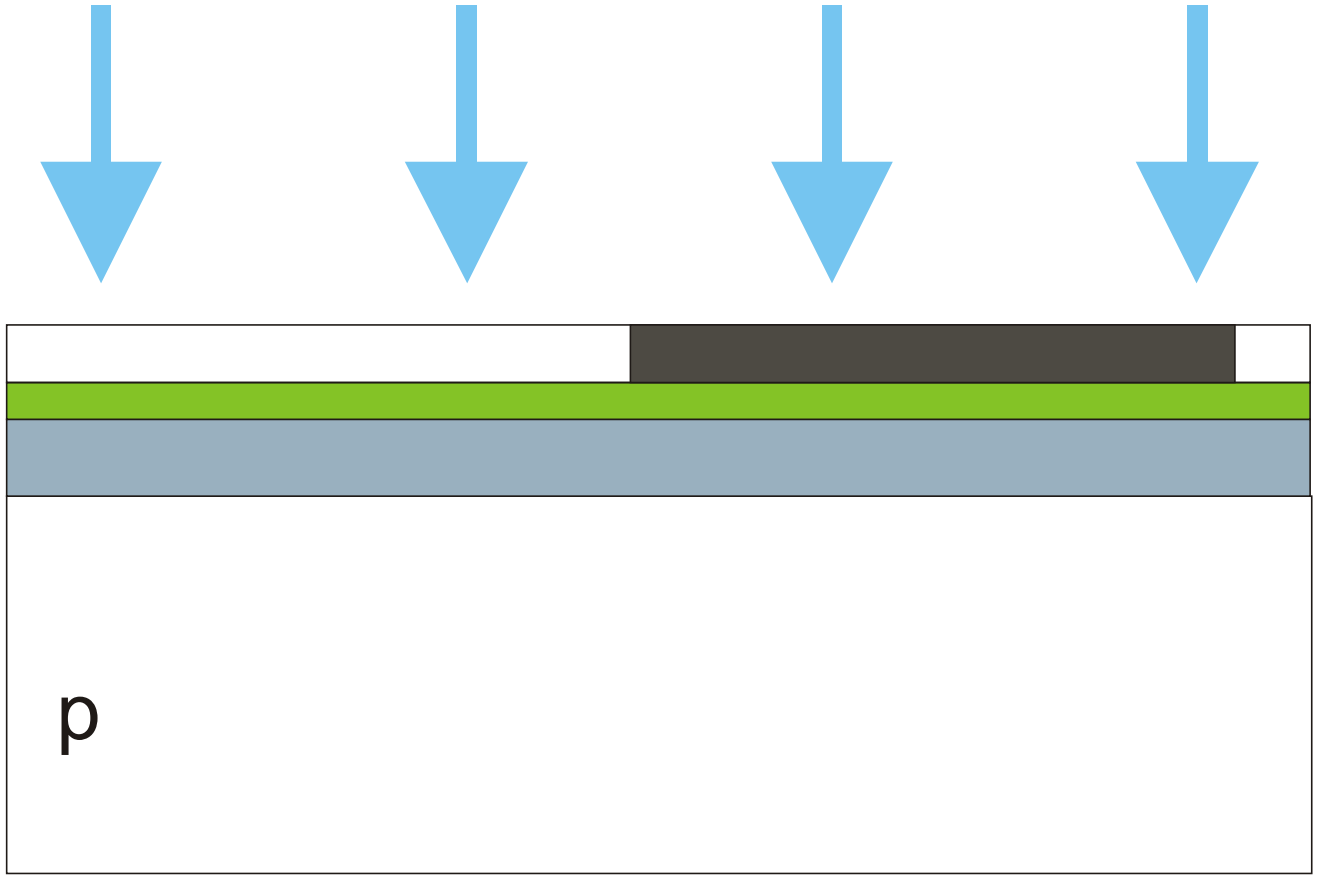
Substrate Oxidation



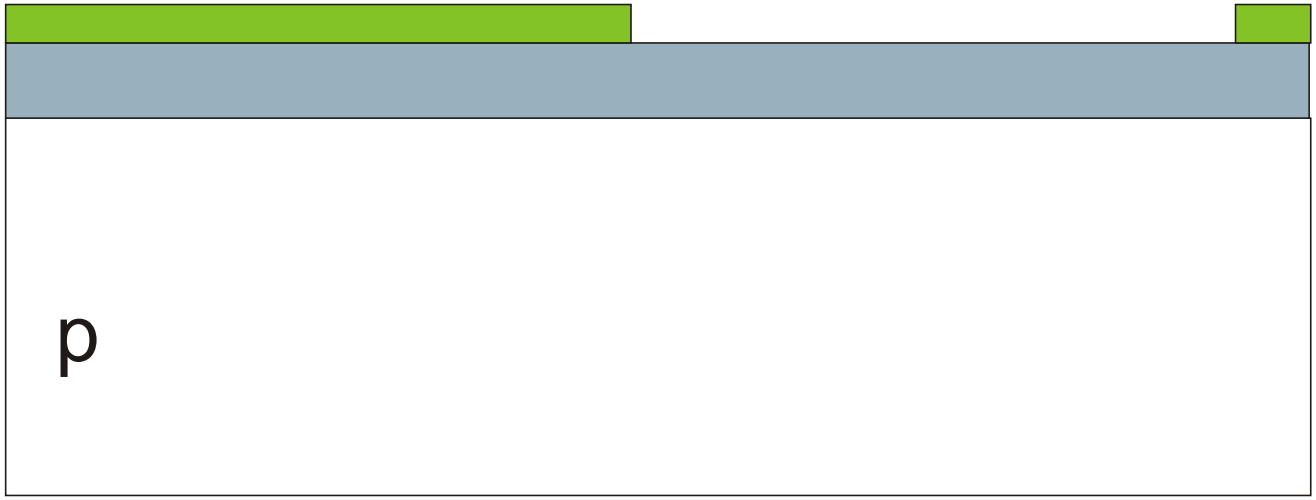
Deposition of Photoresist



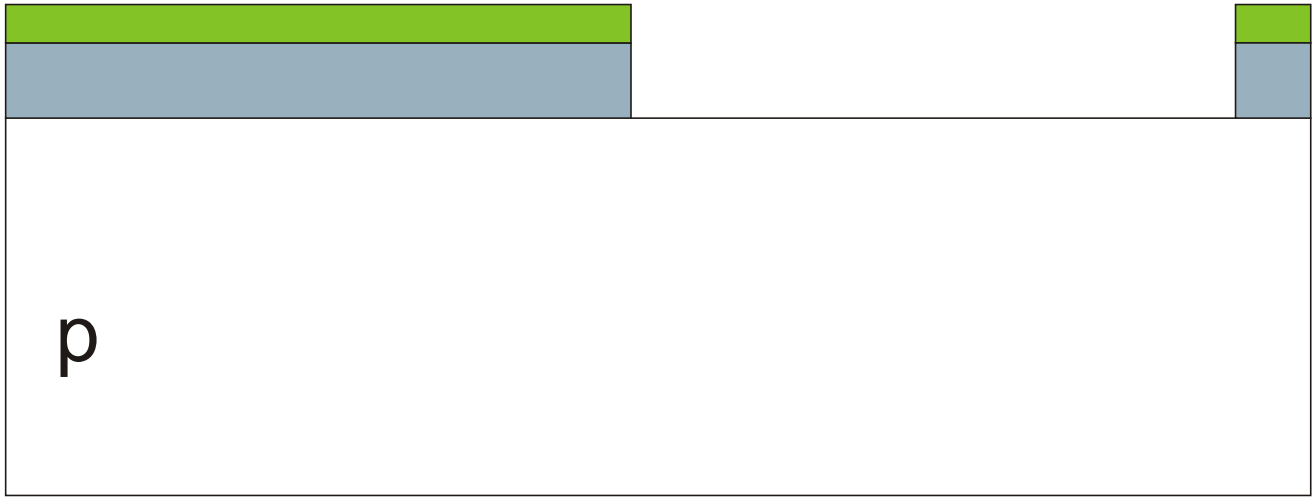
Masking and Projection



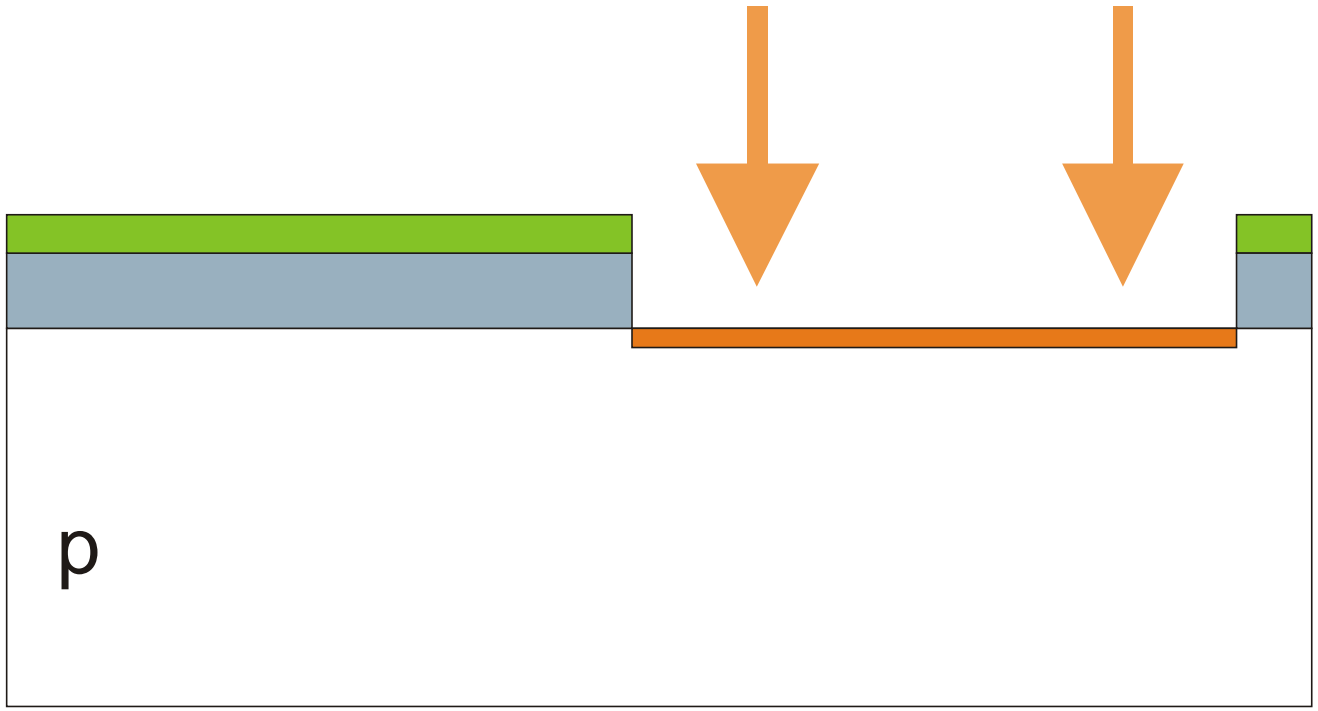
Developing of Photoresist



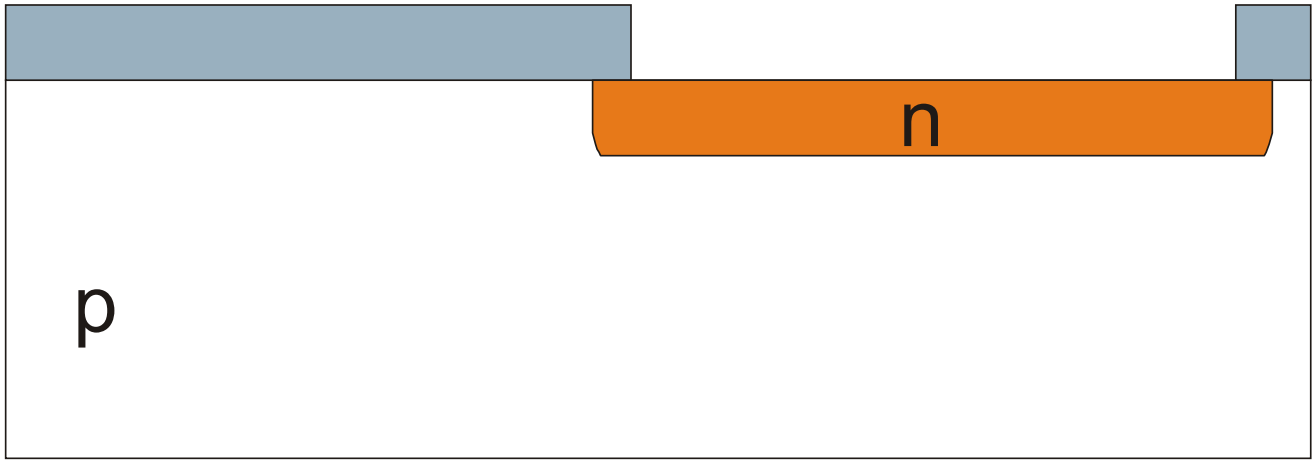
Oxide Etch



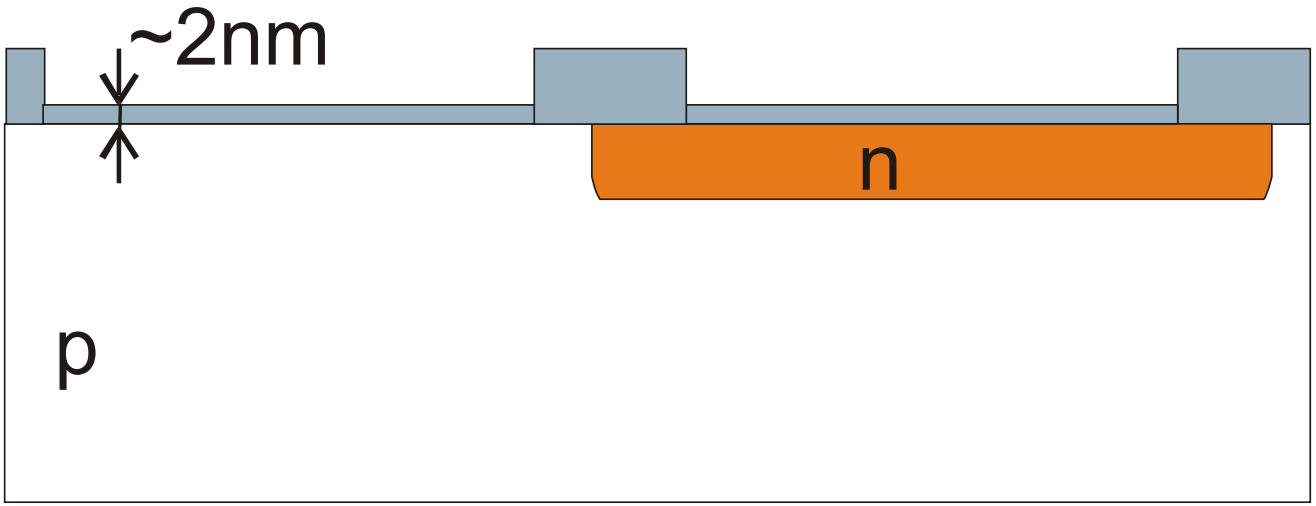
Ion Implantation



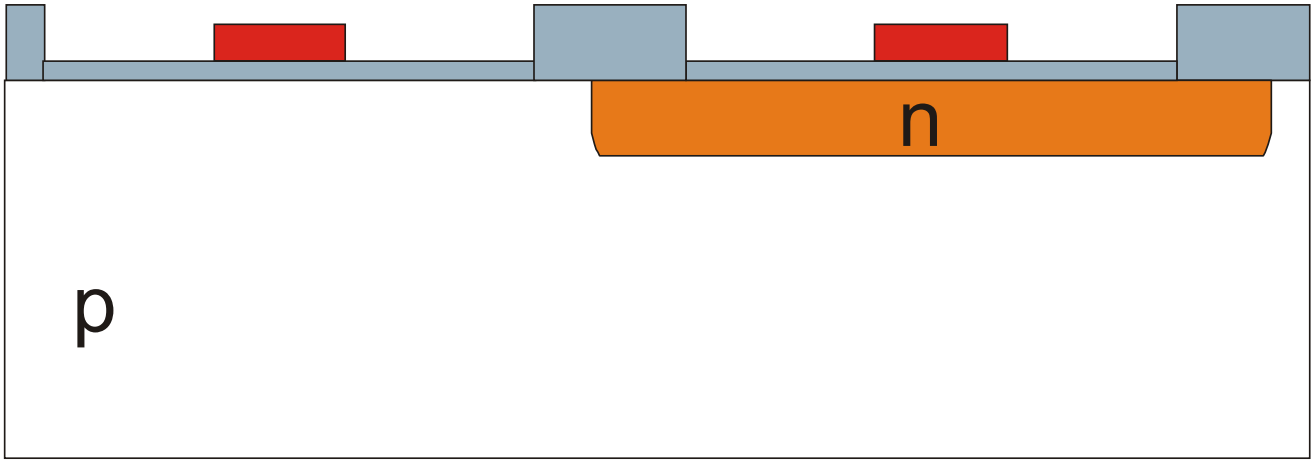
Annealling / Rediffusion



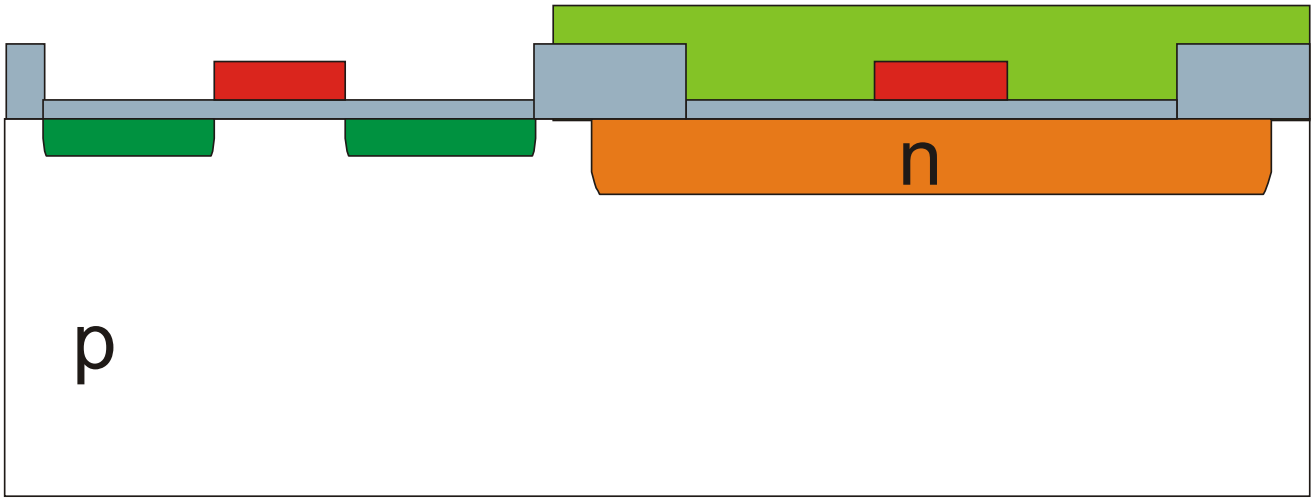
Gate Oxide



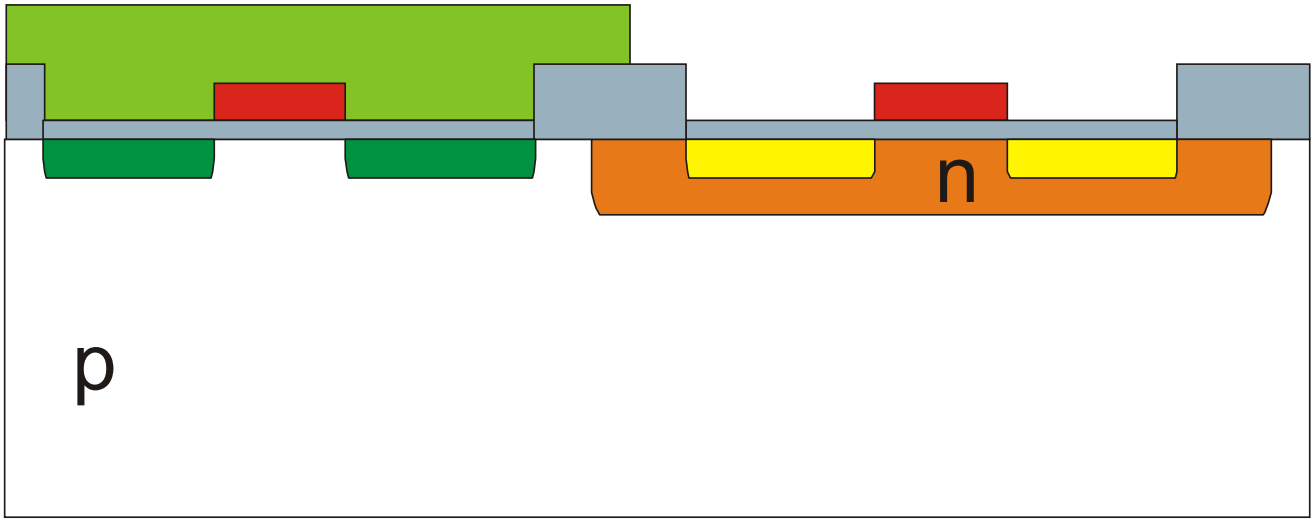
Deposition, Masking and Etching of Polysilicon



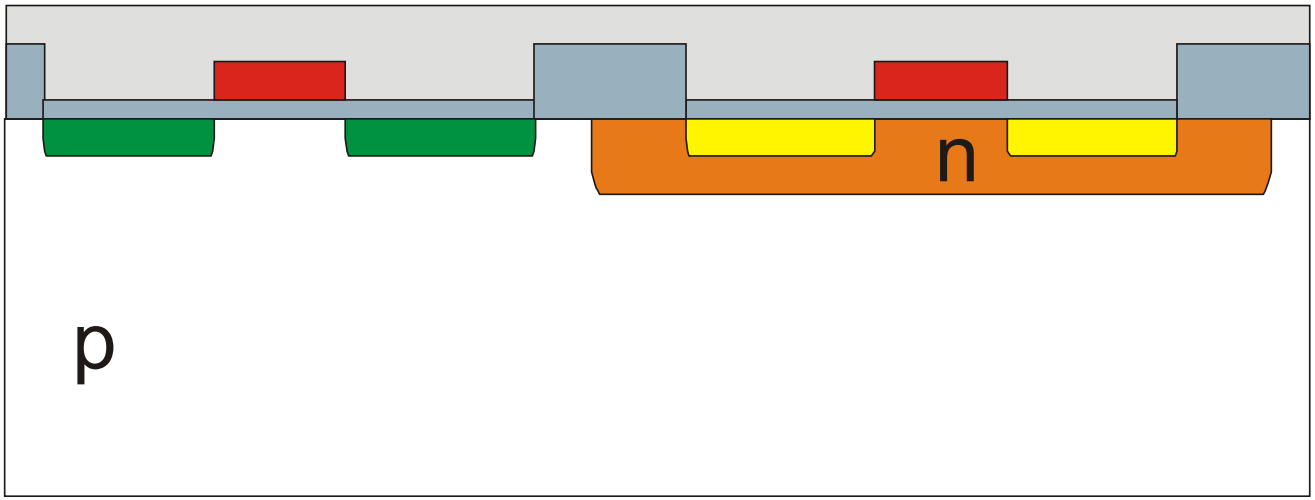
NMOS Manufacturing



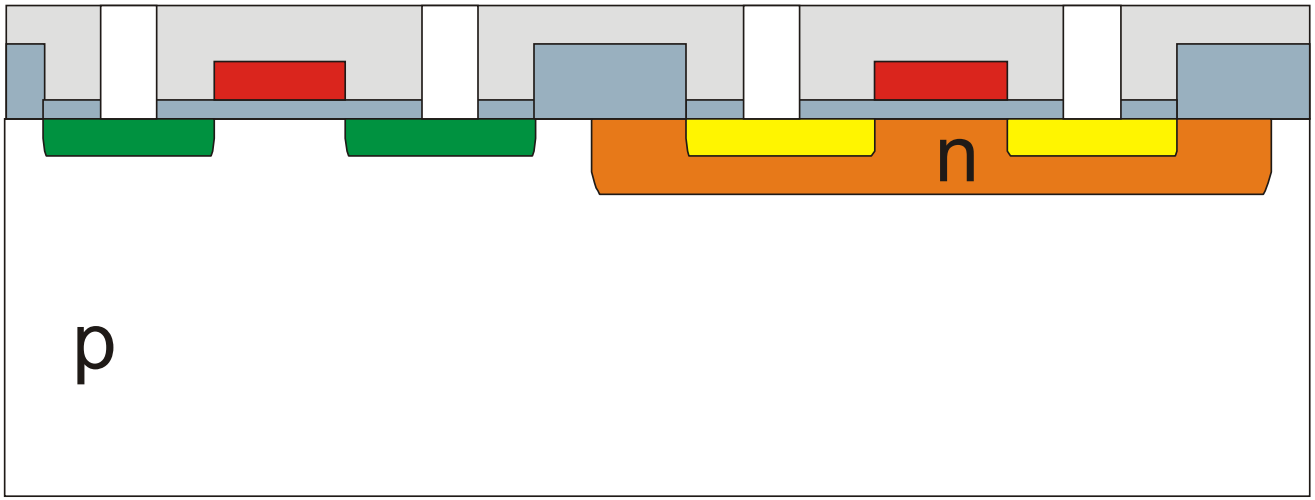
PMOS Manufacturing



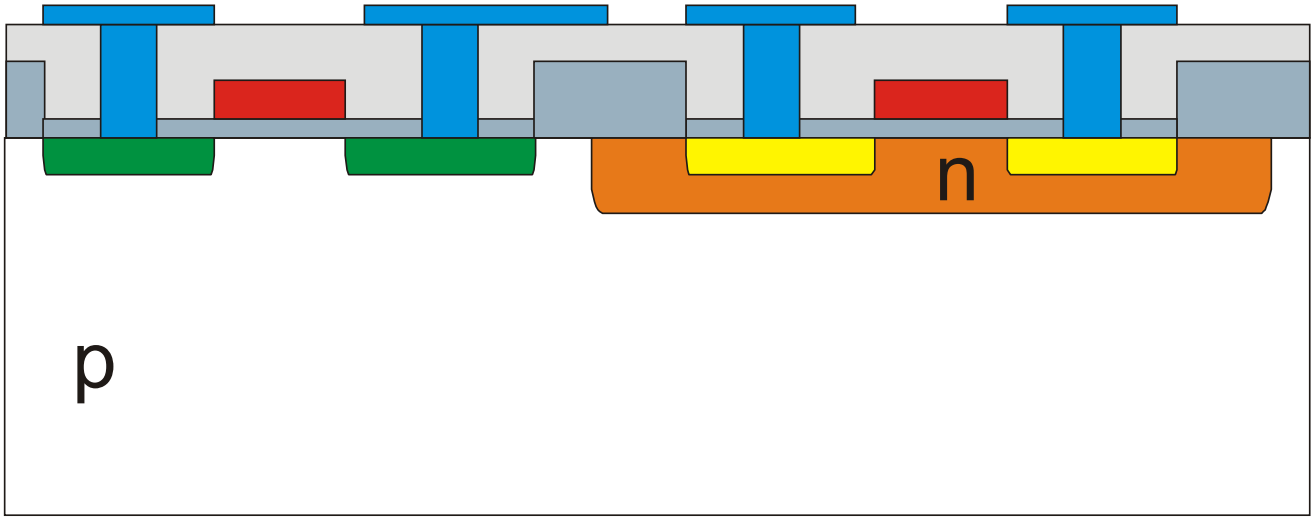
First Insulating Layer



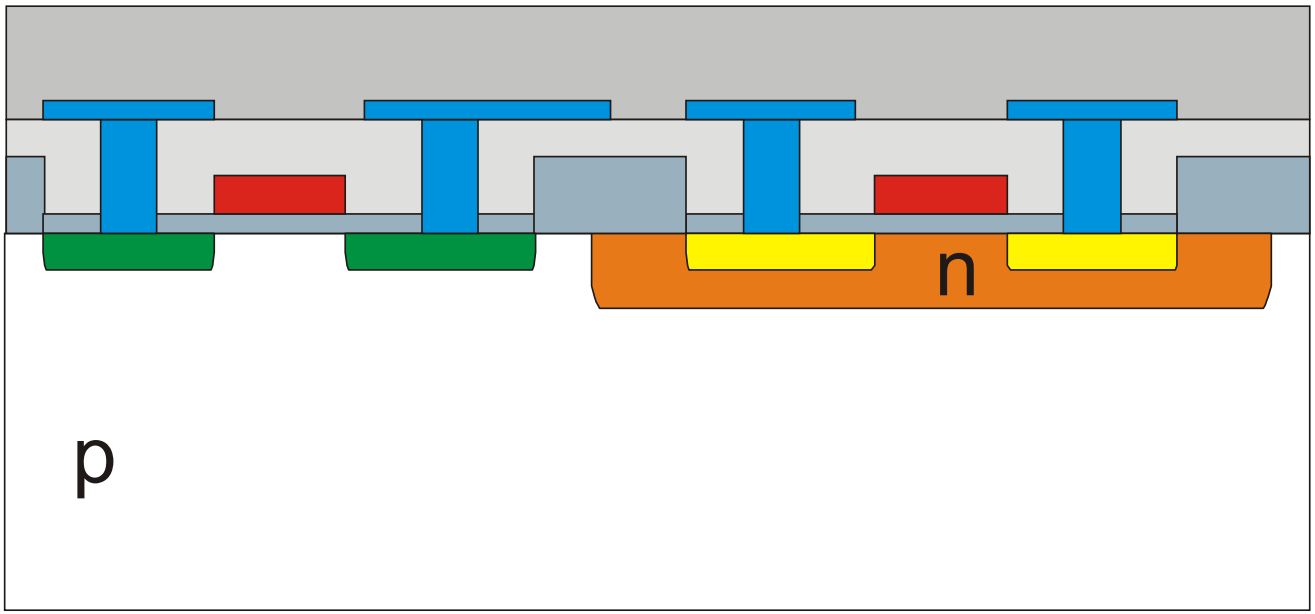
Contact Etch



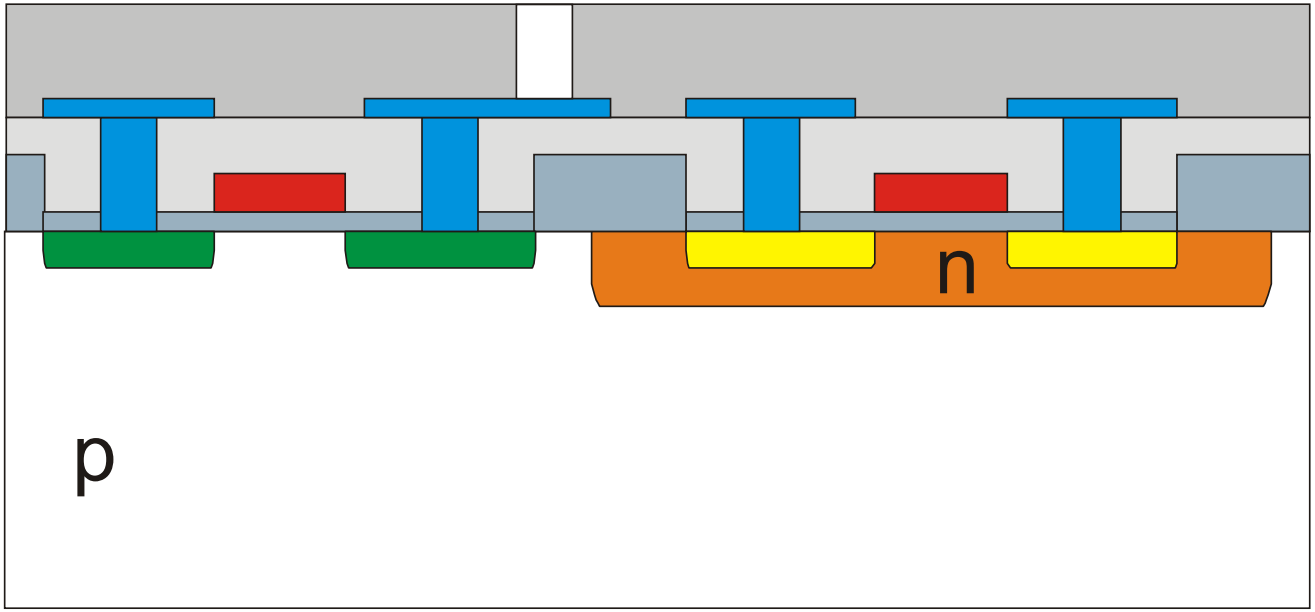
Contacts and Metallization I



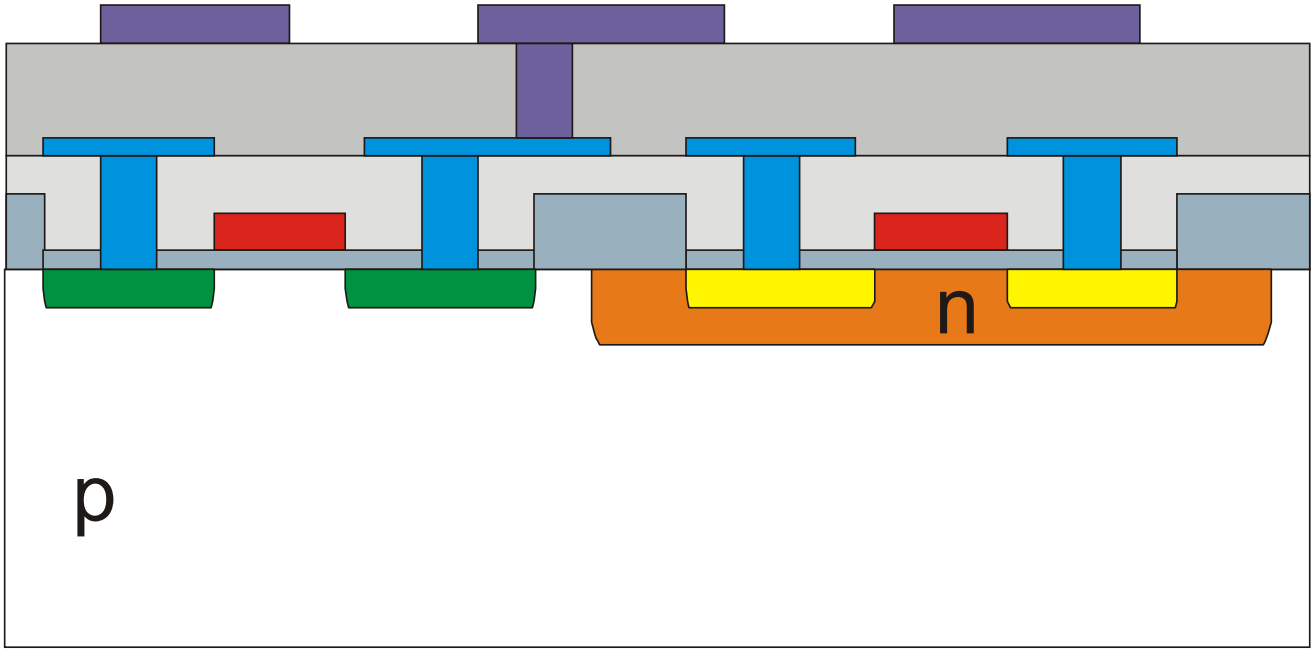
Second Insulating Layer



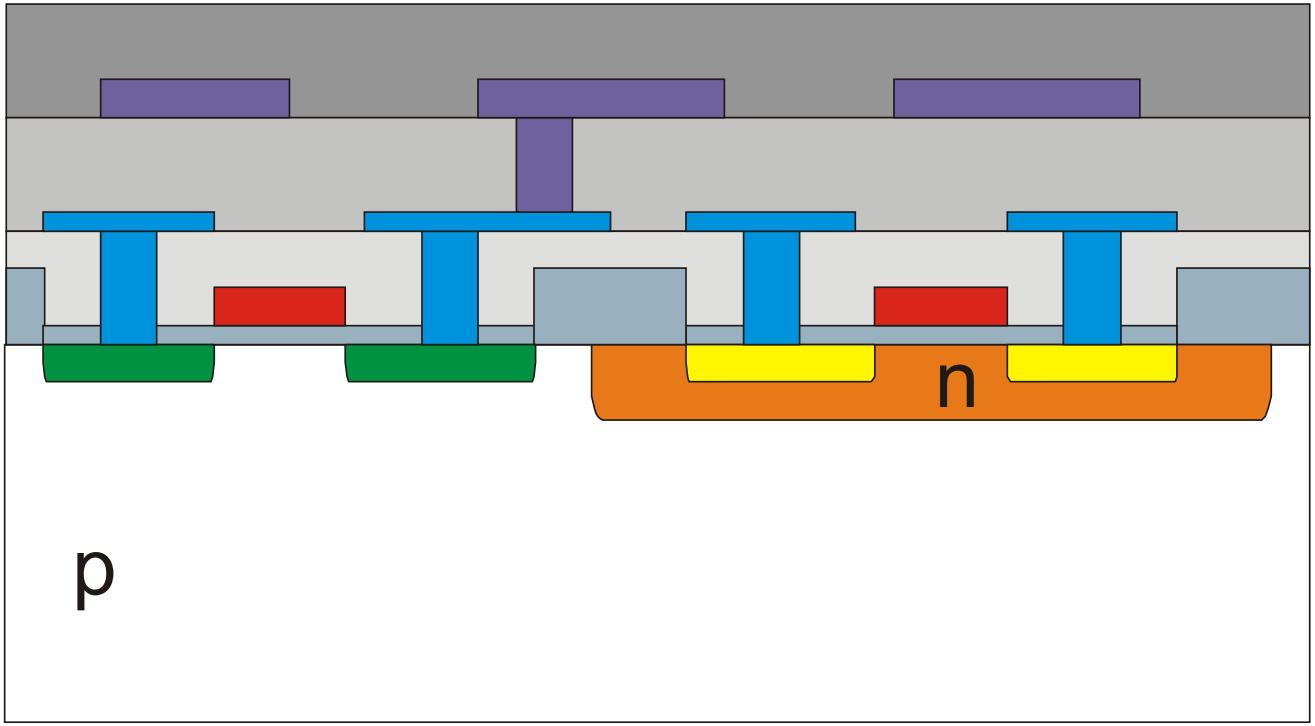
VIA Etch



Vias and Metallization II

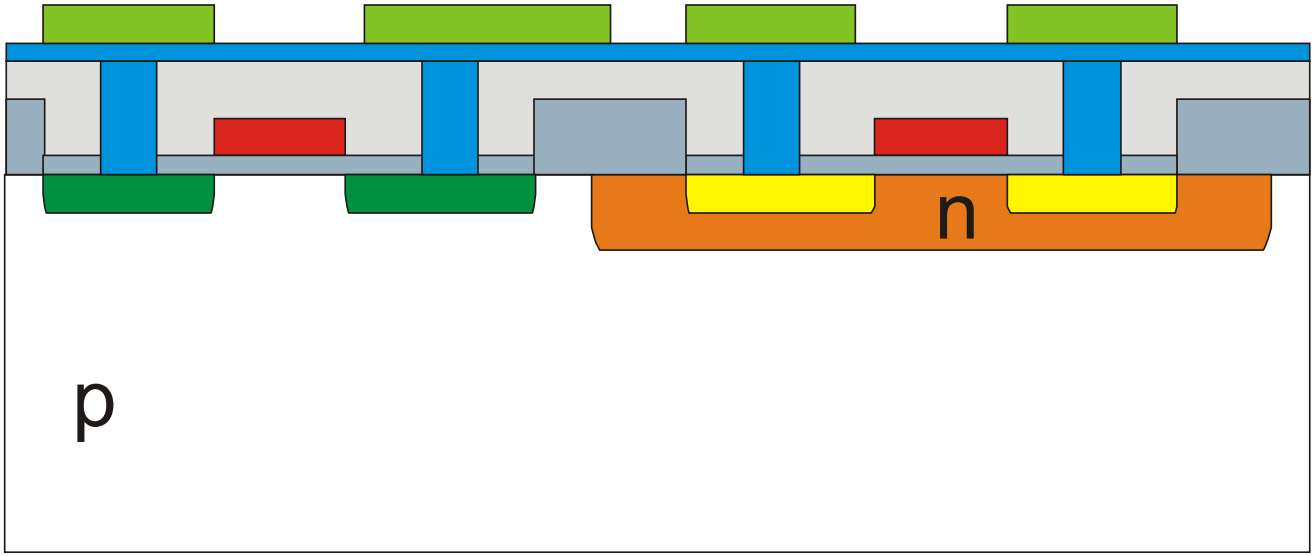


Final Passivation

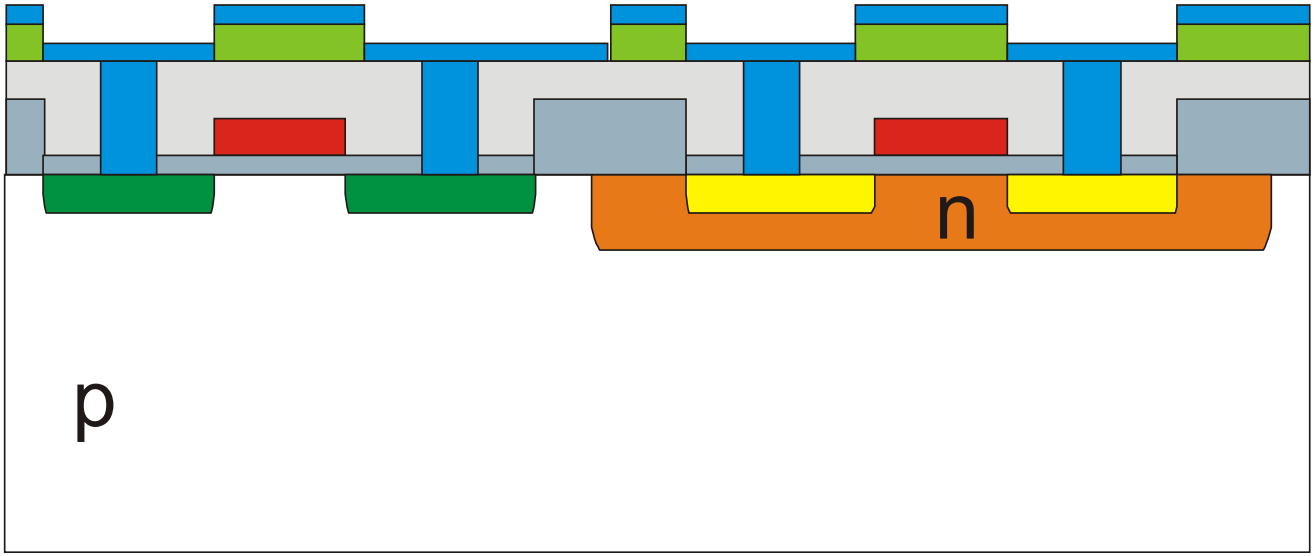


Deposition of Metallic Layers

Etching Away of Excessive Metal



Lift-off

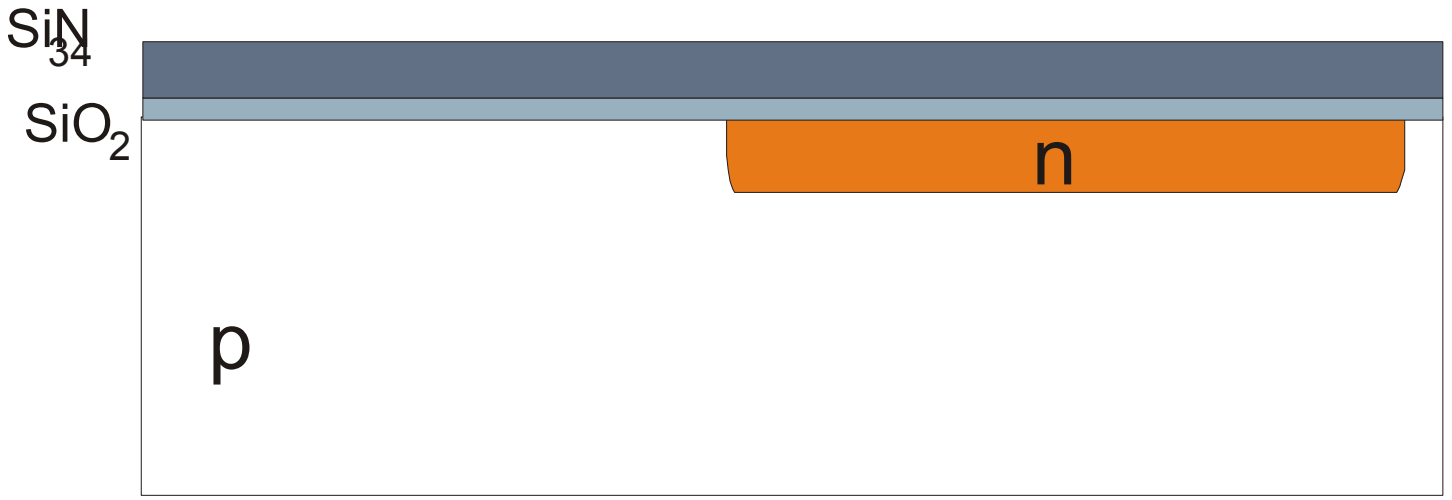


Metal-Semiconductor Contacts

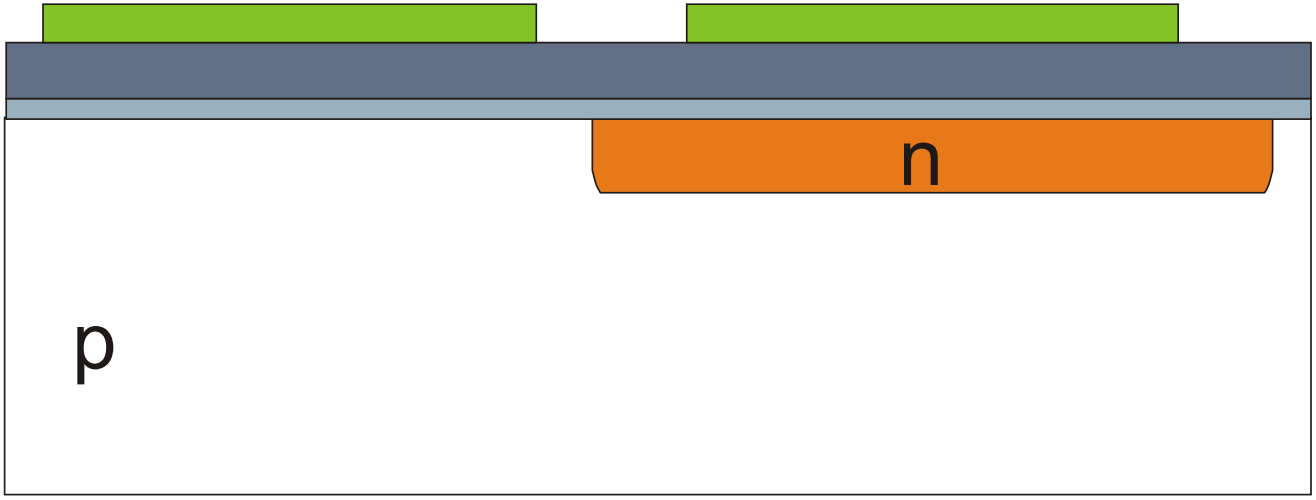
- Drain and source pins
- Substrate and well bias
- Always to heavily doped semiconductor
  - low ohmic resistance
  - no Schottky junction

LOCOS Technology

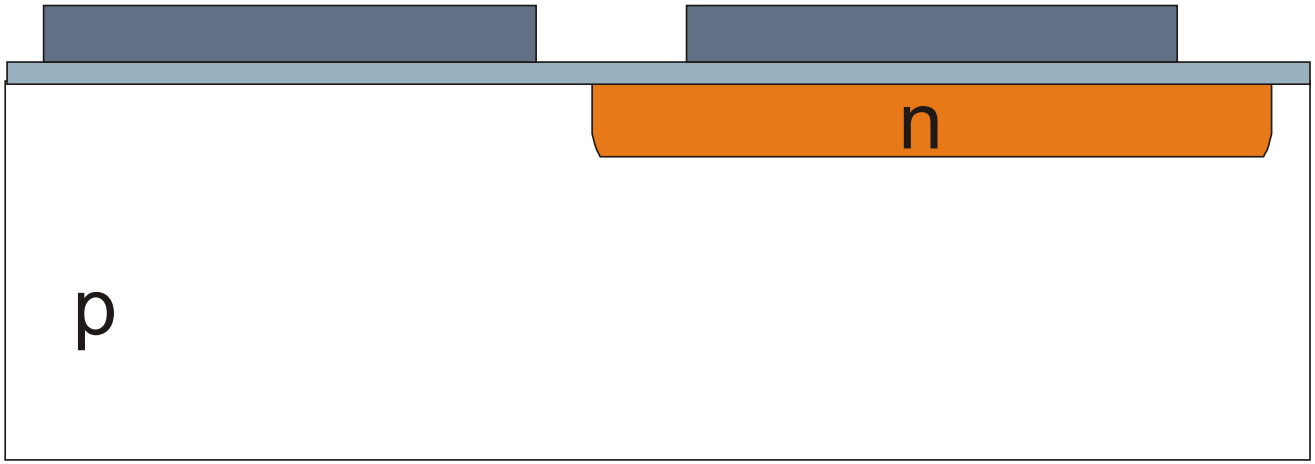
Deposition of Silicon Dioxide and Silicon Nitride



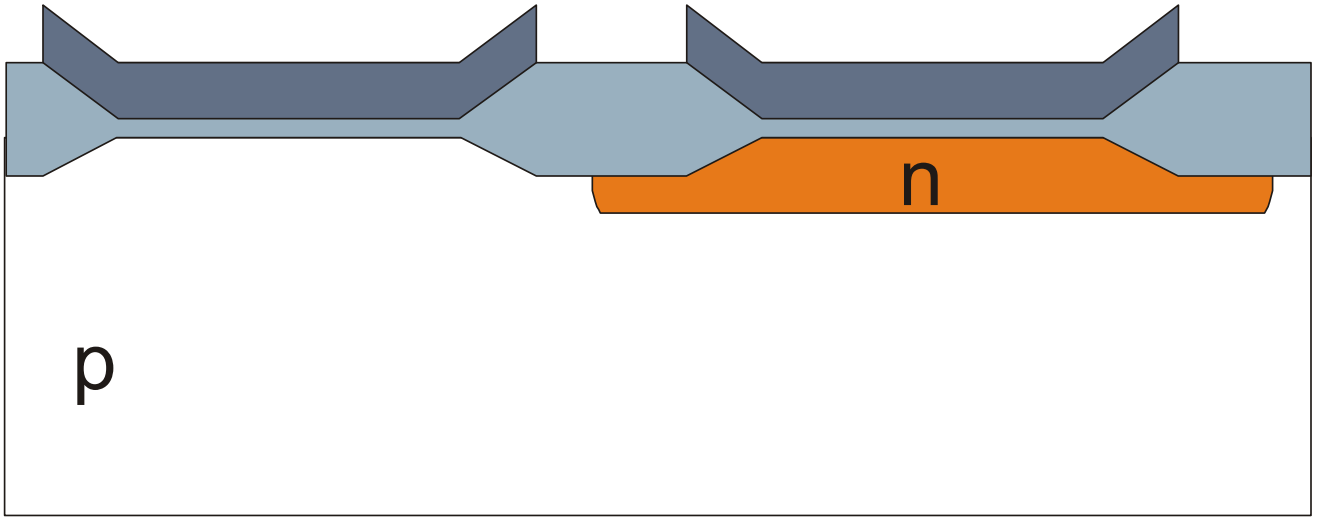
Deposition, Masking and Etching of Photoresist



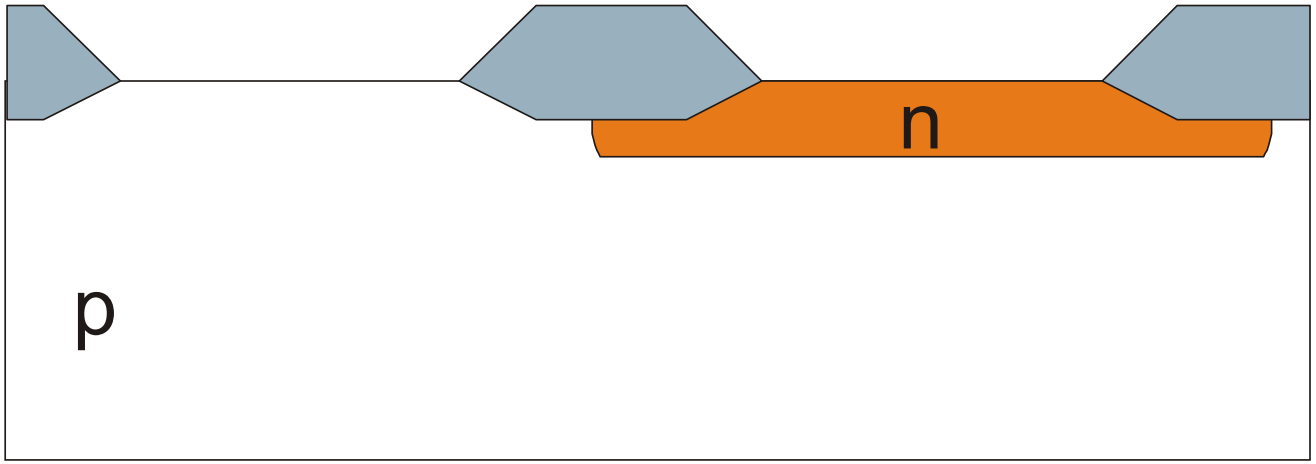
Etching of Nitride and Removal of Photoresist



Field Oxide Manufacturing

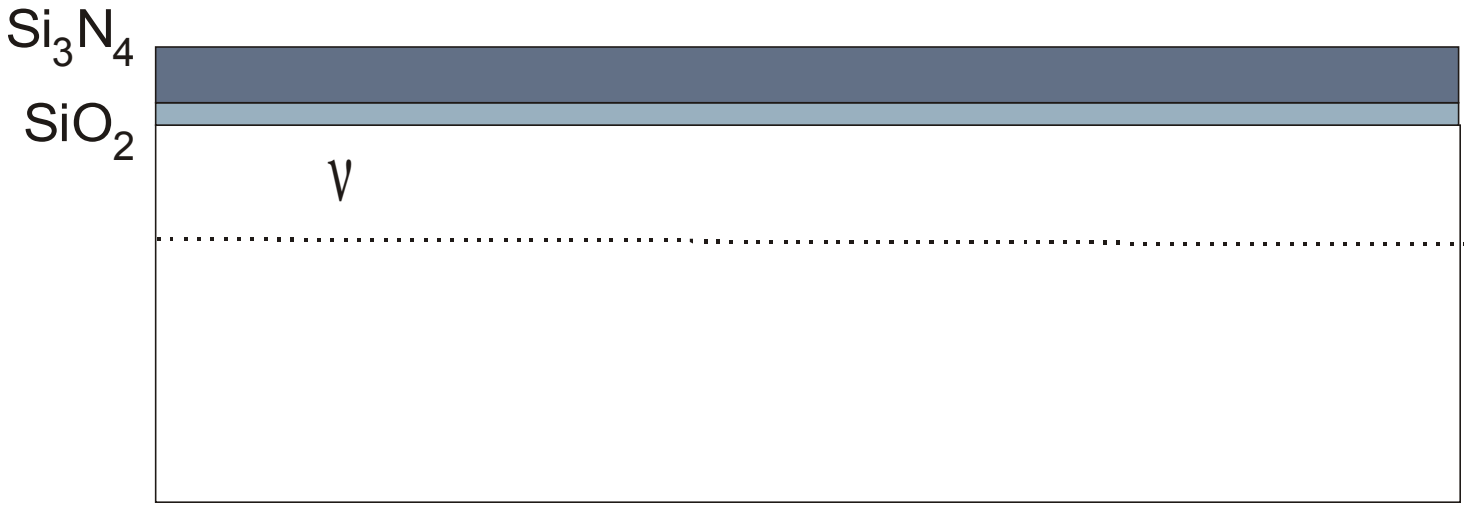


Removal of Nitride and Thin Oxide

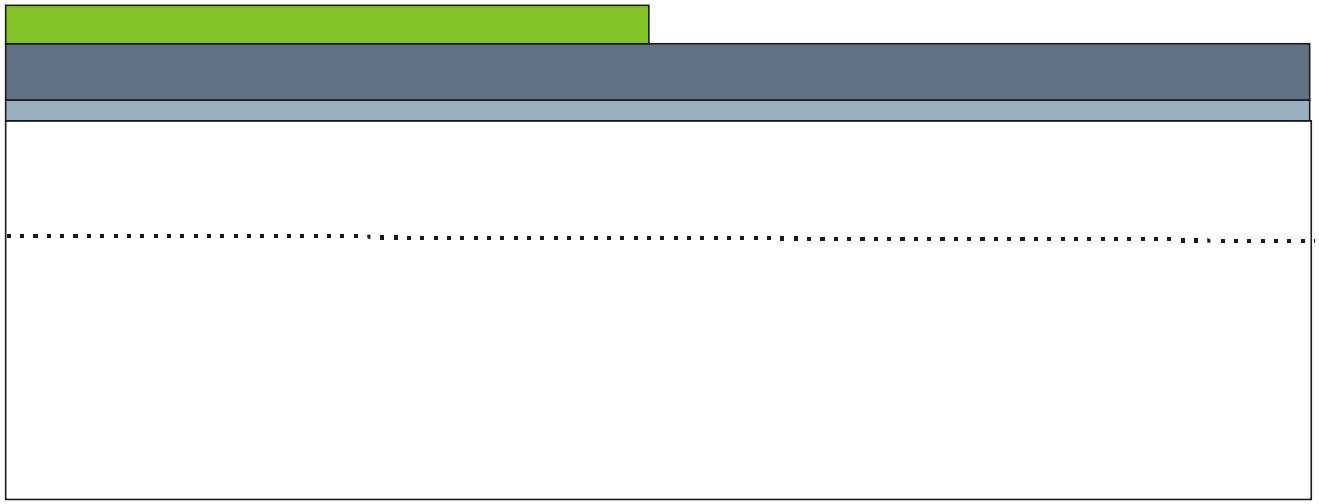


Twin-Well (Twin-Tub) Technology

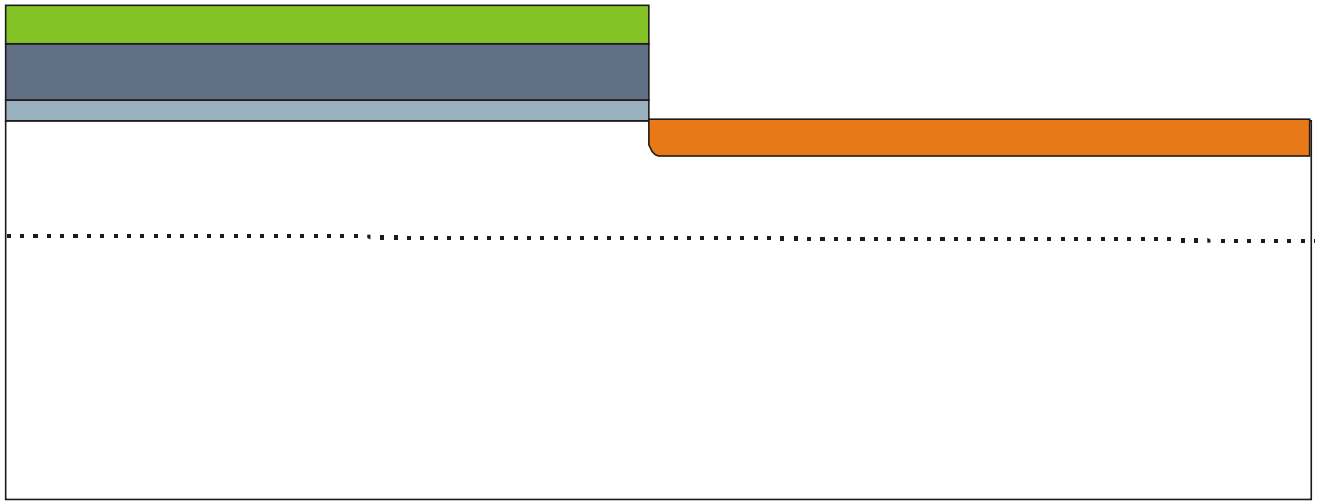
Epitaxial Layer Covered by Oxide and Nitride



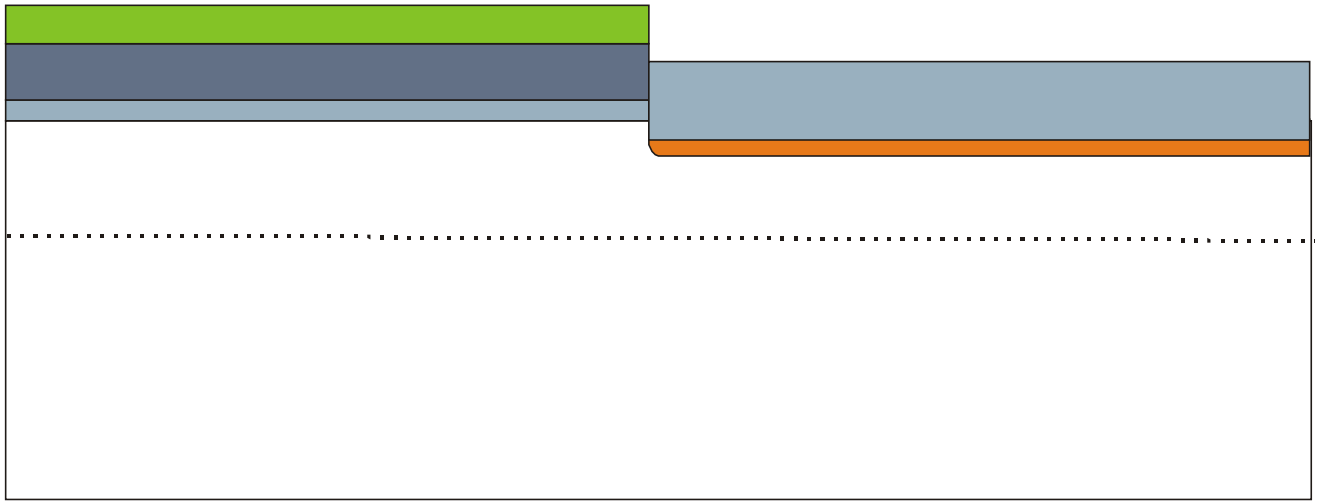
Photoresist Deposition, Projection, Developing and Removal



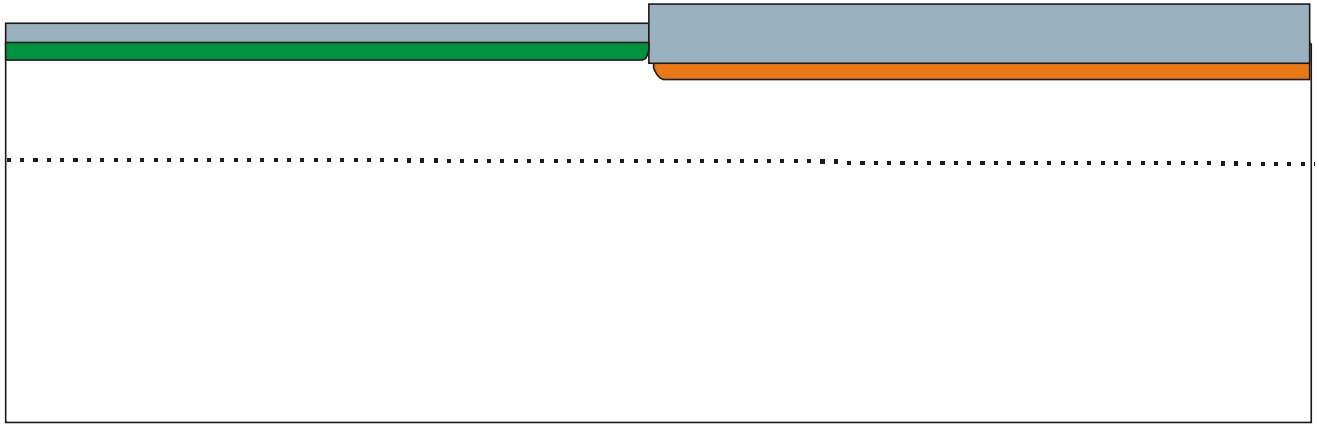
N-Well Implantation



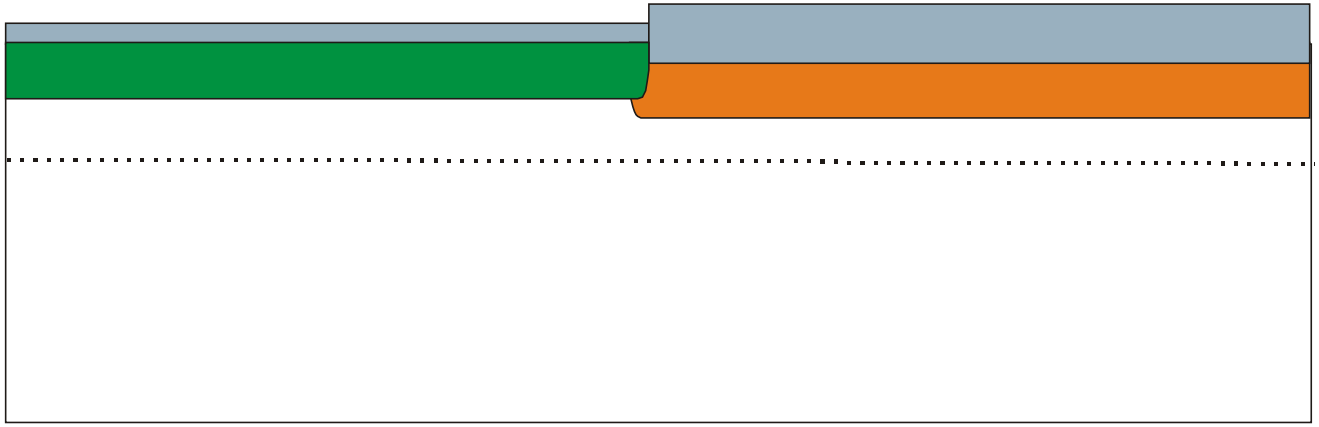
Thick Oxide



P-Well Implantation

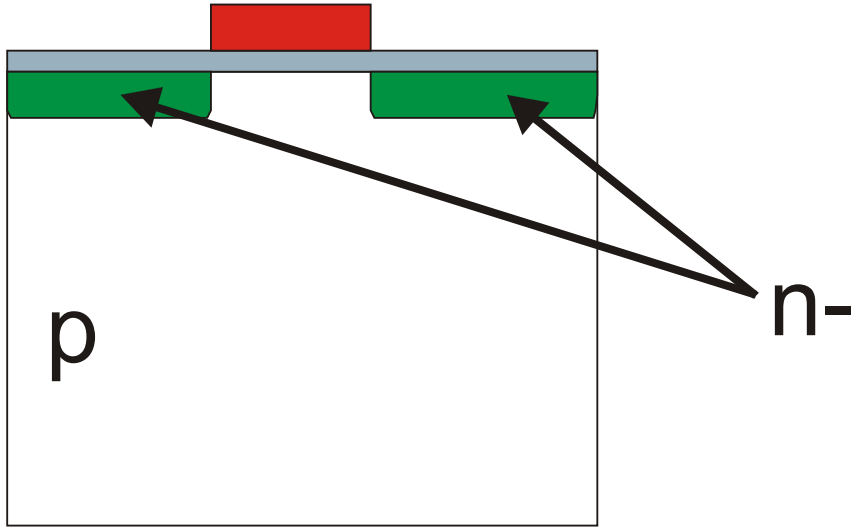


Annealing / Rediffusion

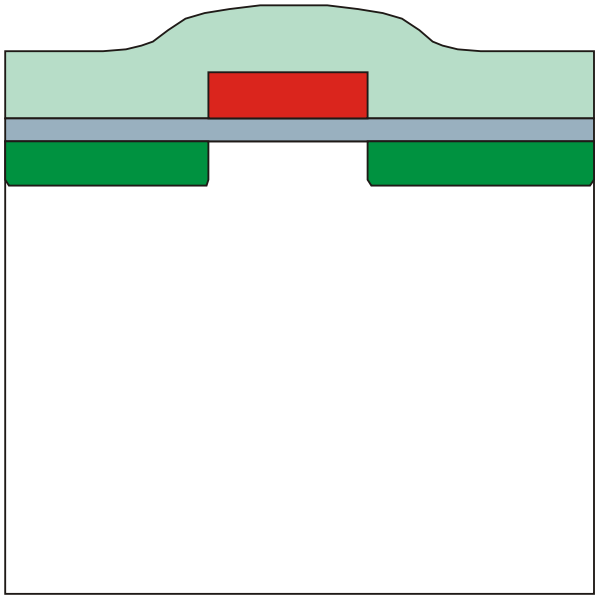


Lightly Doped Drain (LDD) Transistor

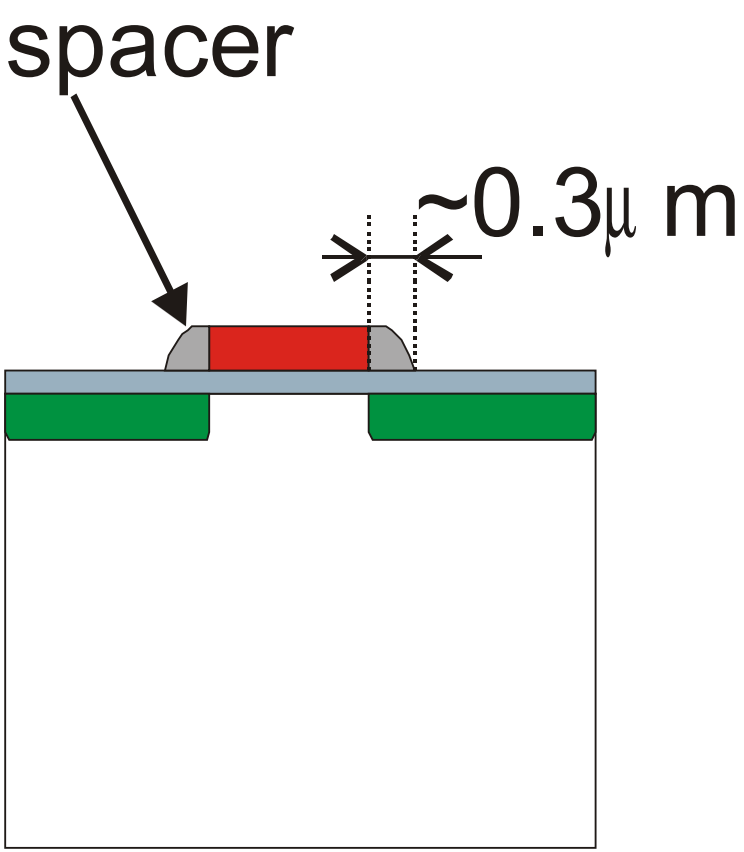
Implantation of Lightly Doped Drain and Source Areas



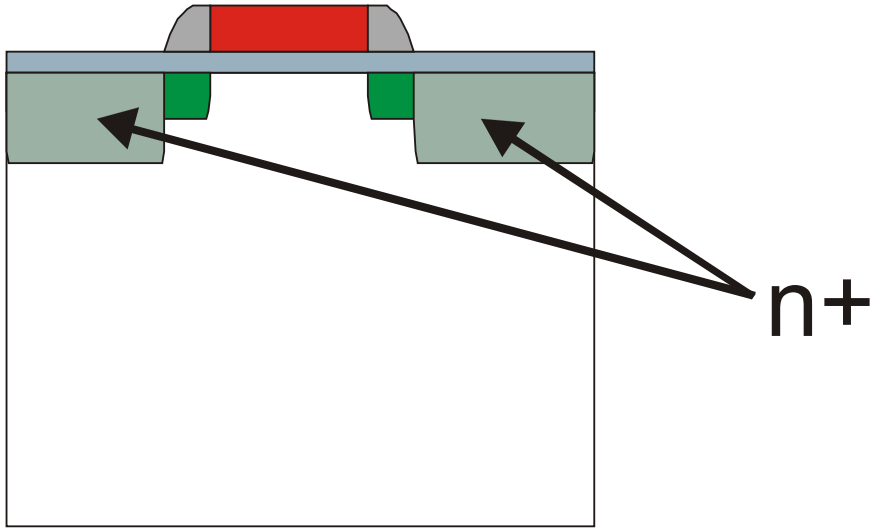
CVD of SiO_2



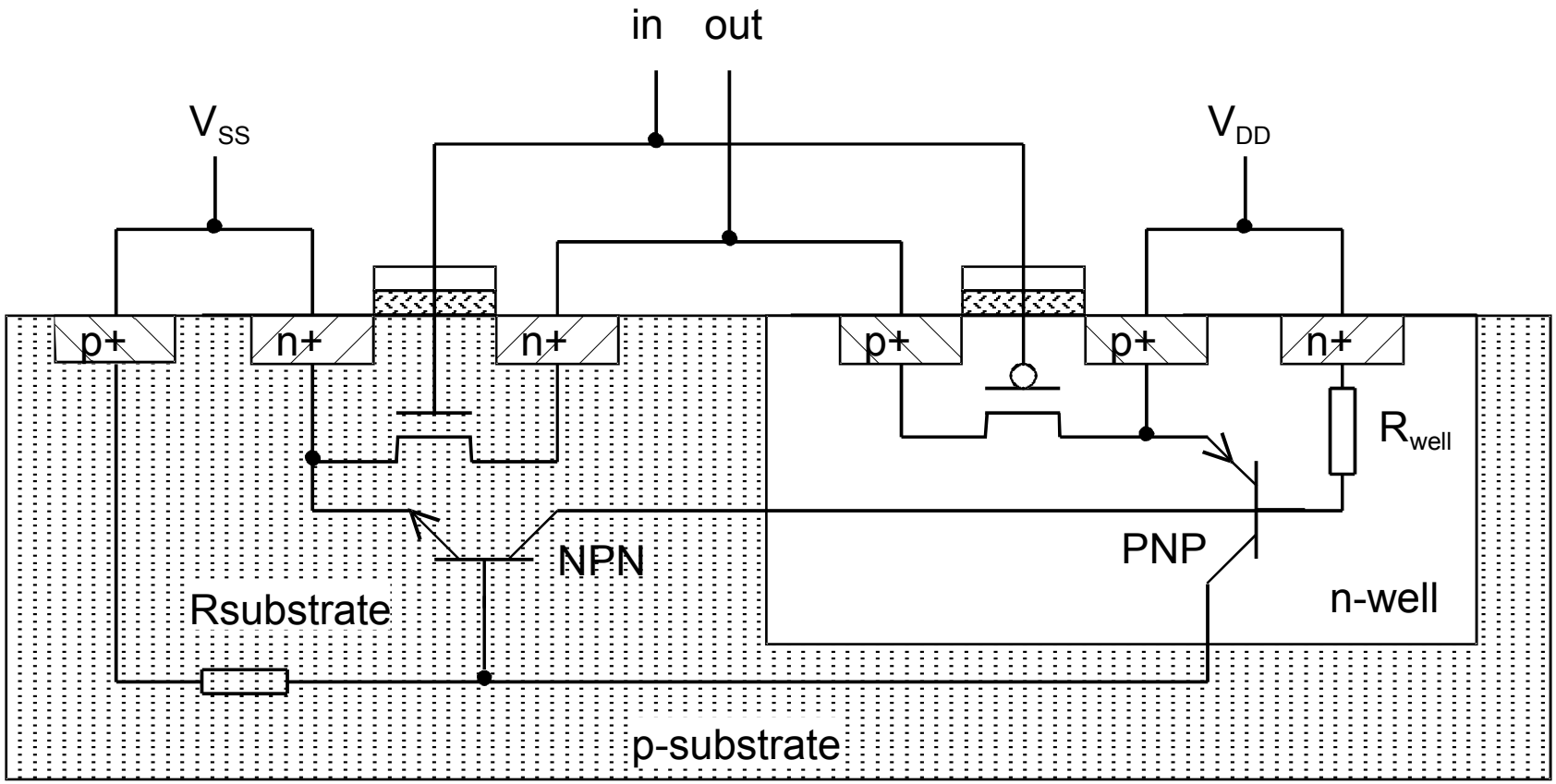
SiO_2 Etch



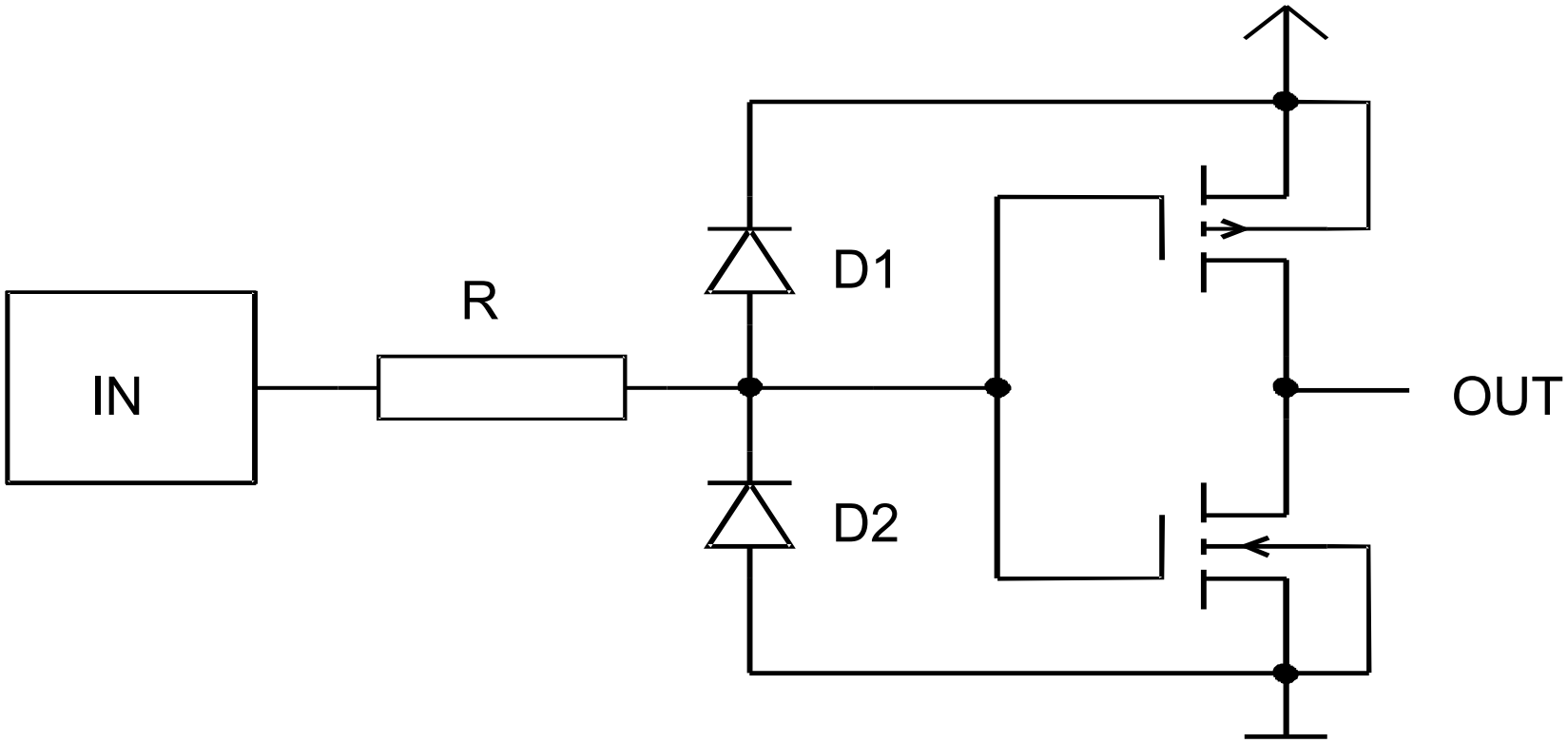
Drain and Source Implantation



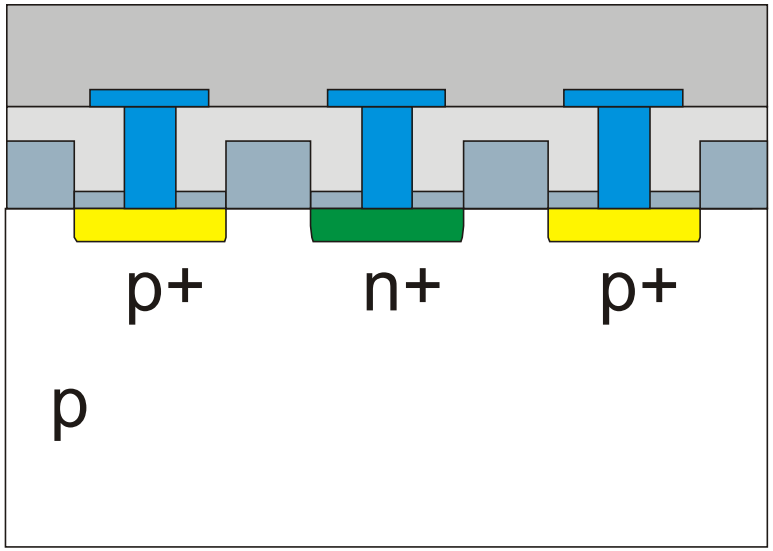
Latch-up

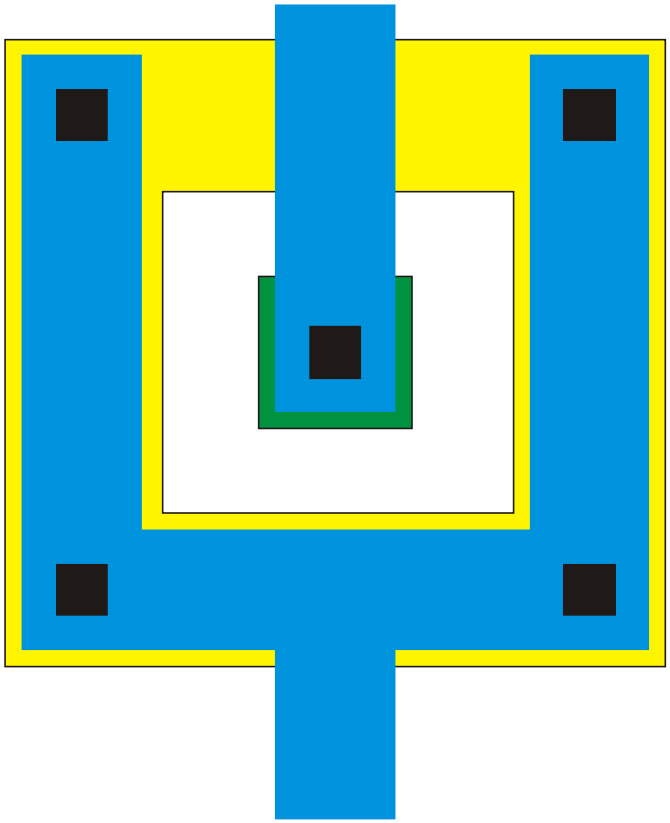

in
out
V_{SS}
V_{DD}
p+
n+
n+
p+
p+
n+
R_{well}
NPN
PNP
Rsubstrate
n-well
p-substrate

Input Protection Circuit



n+/p Diode





p+/n Diode